USE OF THE GLOBAL COMMUNICATIONS LINES IN THE HOMOGENEOUS MACHINE

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1. Introduction

This document is concerned with some functions that will be incorporated into the read only memory on each processor of the homogeneous machine. The software in the read only memory is the only software guaranteed to be functional at all times. After power on or after an errant user program causes damage to the system, the contents of writable memory will be unreliable.

The functions that must be performed by this hardware include setting up a system after application of power, processing parity errors or other hardware problems, debugging faulty user programs, and refreshing of the dynamic memories.

The basic processor hardware includes some global control and communication functions. Specifically, the dedicated host is able to control the reset and non-maskable interrupt lines to all the processors simultaneously. Three general input lines are provided that are settable by the dedicated host and readable by each processor. Five open collector output lines are settable by each processor, and the wired-and function of these lines can be read by the dedicated host. Judicious use of these 10 signals must be sufficient to implement all the desired control and diagnostic functions.

2. Use of the Non-Maskable Interrupt

The non-maskable interrupt provides a reliable method of invoking read only code[1]. The 8086 processor will respond to a NMI interrupt whenever

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[1] Assuming that the NMI vector is in read only memory.

the NMI line goes high for more than two clock cycles. The response will occur regardless of whether another interrupt (NMI or otherwise, software or hardware generated) is being processed. Response to the NMI will occur at the completion of the instruction executing in a processor when the interrupt is detected. This time may vary, but is guaranteed to be small.

Since the global data lines are controlled only by the dedicated host, they can be used to reliably communicate messages to all processors simultaneously[2].

The global open collector lines can be used for communicating messages to the dedicated host under somewhat restricted conditions. Since the global open collector lines are common to all processors, only one processor can meaningfully communicate with the host at once. This can be assured if three conditions are met: 1) no hardware failures exist, 2) user programs are not running, and 3) processors can distinguish between themselves[3].

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[2] The global data lines can be effected by a hardware failure in any of the processors in the array, and hence other methods must be provided for locating such failures.

[3] Let us clarify this point. All processors have previously been assumed to be identical, and the global communication does not distinguish between any processors. Under these conditions a processor cannot know when a message is directed to it or to another processor, and therefore cannot know that it is the unique processor intended to return a message. Other methods will have to be worked out to give each processor a unique identification.

3. Control Functions

The following convention is proposed for communicating control functions to the processors: a non-maskable interrupt will be initiated with the three global data lines set to a one-of-eight function code. The following function codes will be implemented:

Refresh. Causes the dynamic memories to be refreshed. Under normal operation this will be executed every 4 mS.

Restart Normal. Causes the software to startup the system in normal mode. Normal mode includes allocating all of the memory and enabling all communication facilities.

Restart Minimal. Causes a software startup where the previous state of the system is effected as little as possible. This would be used when a user error is detected and it is desired to stop execution of the user program but to be able to examine the previous registers and memory. Only a special diagnostic portion of memory is used.

Check. Causes the monitor to verify the consistancy of as much of the system as possible. This will include checking magic numbers on storage records, verifying the executable process queue, and possibly verifying checksums on read only segments.

Bit 0. Receives a 0 bit over the global channel, see secton on global serial communication.

Bit 1. Receives a 1 bit over the global channel, see secton on global serial communication.

User A. User function A.

User B. User function B.

Note: Although the **refresh** function was the only function described as refreshing the dynamic memory, all other functions may do this also.

4. Global Serial Communication

A general purpose, but low bandwidth, broadcast communication can be implemented through the functions **bit 0** and **bit 1**. These functions will be executed in groups of eight where each processor will accumulate the eight 0 or 1 bits into a byte. After the eighth bit has been received the byte is made available on the global data input channel. A diagnostic monitor can be written that processes input from this channel.

5. Defeat of Functions for Special User Operations

In some cases the user may wish to have extensive control over the hardware. This control will be provided in the following manner:

- The NMI interrupt will not be available to the user except through the two unimplemented codes.
- Other interrupts are generated by the 8259A interrupt controller that has a selectable interrupt vector. The operating system will initialize these vectors to point to vectors in read only memory that refer to operating system routines in read only memory. The user program is free to change the vectors to point to a second table in memory, however. This table will vector all interrupts to a fixed area in read/write memory that the user presumably has initialized with his own routines.