Erik DeBenedictis
Internal Transfer Rate

3' Ribbon Cable  
300" = 25' Ribbon Cable

900 ns / cycle

2000ns / cycle
DH280 Board

O3M01 X1
O3M02 X2

O3M15 GND
O3M16 GND

O3M CC
- 510Ω
- 510Ω
- 0.02Ω
- 50kΩ
PROM8

Does checksum of its prom (800-FFF) and prints on terminal. Repeats.

Should print 954B

PROM0

Does checksum of PROM0 (0-800) and prints on terminal. Repeats.

Check with PROM burner for verification.

RAM4

Does ramcheck of ram at 4000-7FFF. Writes incrementing 16 bit patterns and compares back. Starting 16 bit value is printed each iteration.

If fail is found program checks S1 to continue
S1 up ⇒ continue
S1 down ⇒ wait

RAM5

Same as RAM4 but for RAM 8000-BFFF

RAMx

Same as RAM4 but for RAM 4000-BFFF
ECHO

Outputs message. Then inputs from terminal and echoes character plus one.

I/O check: $S_{10}$/0

<table>
<thead>
<tr>
<th>Ch</th>
<th>Rx/DA</th>
<th>Tx/DA</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>B</td>
<td>28</td>
<td>26</td>
</tr>
</tbody>
</table>

IMPORTANT

RAMALL

Checks all RAM ($4000$-$BFFF$). If an error is detected, the syndrome is printed. $S_1$ up ⇒ continue on error, $S_1$ down ⇒ stop on error.
EMON for DH280

NMICNT 42FF
OUTBYT 4301
-I078 <=> Reset fifos
TIMING
(Forrest it)

MAIN BOARD

8288 -AEN should be GND, not 5V
-RAS should come from -A17
-PROM should come from A17
RAM address Power Supply Backward
IO word addressed - change decoders to A4, A2, A3 from A4-A1-A2
BASE7 board/wirelist

Discovered logic error on 245, prevented reading external I/O space.

WAS

IS

Base7 is recommended for future designs.
Node OQR needs pullup.
Delay -OQA - OQA is too large.
Delay CK IN \( \frac{1}{2} \) to OR \( \frac{1}{2} \) 25 ns
Please refer to the image for the circuit diagram and the handwritten notes.
TBQ:E Generation

23 January 82
CMOS

2V/div vert
200ns/div horiz

OQR 01602
OQA 01801

OQR 01602
TBQ:E 01803

Traces are centered at zero.

Zero overlap.

No glitch, but signal wiggles a bit.
Data Setup

20 ns/div vert
200 ns/div horizon (multicoloured cable, 1' long)

150 ns setup time

23 Jan 82
Gnos
LS TTL implementation

- Schmitt: 7414 (LS)
- Inverter: 7404 (LS)
- Nor: 14411
- Buffer: 74244 (LS)

**Buffer Effect**

Only change 74C941 for 74LS244!

**Oscilloscope Image**

- 2V/div vert
- 200ns/div horiz

150-225 ns setup time change.

CN05 takes 75 ns longer than LS TTL.
Handshake

2V/1div vert
traces center & bottom
50ns/div horiz

350µs cycle (3 of 4 phases)
TBQE Generation

23 Jan 82
LS TTL

vert 2 V/div (centered)
500 ms/div horiz

Note significant overlap.
No glitch.
Data Setup

IQ9
02F01

IQR
02F04

2V/div vert (centered)
50ns/div horiz

Data Setup -30 ns
Long Cable CMOS interface

60 foot
2v/div vert
5ps/div horiz

Cycle 10µs (3 of 4 phases)
Data Setup

23 Jan 82
Cros Long

2 V/div vert
(cont'd)
5 μs/div horiz

Data setup 2 μs

Dim O2 Flo1

FPR O2 Flo4
<table>
<thead>
<tr>
<th></th>
<th>RX INTR</th>
<th>INT</th>
<th>59A</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>RX INTR</td>
<td>82</td>
<td>81</td>
</tr>
<tr>
<td>1</td>
<td>TX INTR</td>
<td>90</td>
<td>88</td>
</tr>
<tr>
<td>2</td>
<td>TX INTR</td>
<td>91</td>
<td>79</td>
</tr>
<tr>
<td>3</td>
<td>TX INTR</td>
<td>70</td>
<td>79</td>
</tr>
<tr>
<td>4</td>
<td>RX</td>
<td>69</td>
<td>79</td>
</tr>
<tr>
<td>5</td>
<td>RX</td>
<td>68</td>
<td>76</td>
</tr>
<tr>
<td>6</td>
<td>RX</td>
<td>65</td>
<td>74</td>
</tr>
<tr>
<td>7</td>
<td>RX</td>
<td>65</td>
<td>74</td>
</tr>
</tbody>
</table>
An interesting RAM characteristic might be obtained by examining an entire page row.

Locations on each row are separated by 256 addresses (512 bytes). Adjacent rows should be in a known (constant) state to prevent coupling.

We actually examine every 256th byte due to the funny 128 refresh stuff.

Test: Zero 16 rows and analyze only the middle one. Use feedback to adjust delay to exact threshold of one bit and observe other bits. The particular bit of interest is known to drift $0 \rightarrow 1$. 
Feedback model:

Stage 1: exponentially increasing times \(2^n\) until 1 bit observed

Stage 2: successive approx. until convergence

Stage 3: algorithm:

\[
\begin{align*}
\text{init} & \quad \text{jump} = 1 \\
\text{dir} & \quad \text{count from before} \\
\text{if} & \quad \text{direction change from last time then} \\
\quad & \quad \text{jump} = 1 \\
\text{else} & \quad \text{jump} = \text{jump} + (\text{jump}+1) \times 2 \\
\text{end} & \quad \text{if bit} = 1 \quad \text{then count} = \text{count} + \text{jump} \\
\text{if bit} = 0 & \quad \text{then count} = \text{count} + \text{jump} \\
\quad & \quad \text{dir} = \text{bit}
\end{align*}
\]

Output row not tested:

Results: particular unit

5F8E on screen COUNT 0578 820A08008020BA heat gun 20"
CPU fails, probably just hot!

Might be unreliable?? Can't tell.

4393 8A0A2B00002888
458E 8A0A2B00002888
<table>
<thead>
<tr>
<th>Other unit</th>
<th>First unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA9F</td>
<td>2A2A0222A2A880</td>
</tr>
<tr>
<td>IAAD</td>
<td>AA2A0222A2A880</td>
</tr>
<tr>
<td>IAGF</td>
<td>2A2A0202A2A880</td>
</tr>
<tr>
<td>1952</td>
<td>AA2A0202A2A880</td>
</tr>
<tr>
<td>1986</td>
<td>2A2A0222A2A880</td>
</tr>
<tr>
<td>145B</td>
<td>2A2A0202A2A880</td>
</tr>
<tr>
<td>414A</td>
<td>0A0A2800002088</td>
</tr>
<tr>
<td>4188</td>
<td>8A0A2800002888</td>
</tr>
<tr>
<td>429B</td>
<td>8AYA280080289A</td>
</tr>
<tr>
<td>3FB3</td>
<td>0A0A2800002888</td>
</tr>
<tr>
<td>3937</td>
<td>8AYA2800002888</td>
</tr>
</tbody>
</table>
Speed Check

65,000 packets in 6 sec
10 K packets/sec
10K-16 160K bytes/sec

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Failure:

- Channel 4, receiver, board 6
- * Cables swapped - no effect
- * Transmit FIFO - no effect
- * 4.956 V original
- 4.817 V still happens
- 5.150 V still happens
- Channel 4, 14001 still happens
- Channel 1, 14CO4 still happens
- * Channel 4 14001 replaced still happens
- * Channel 4 14C14 & 14CO4 still happens
- * Software swizzle of 4&5 still happens
- * Extra software guard still happens

wrong board
Reported RAM problem, CPU #1

Flakiness at the following addresses:

- 55AB
- 67AB
- 57A9
- 60A4
- 58A6
- 5DA3

Program: R, 580h D729

Action: Replace 8288 - no effect

- \( \{ 74L_{100} \} \) with \( \{ 74L_{100} \} \) \( \rightarrow \) 7400/74L5773 (adj 8288) - gone
- 74L500 only - gone
- nothing - still there

- 74L500 with another 7400

- D52B D927
- 74L500 with 74H100 - gone

Old 7400 saved, 74H100 left in

Hit at:

11 FF3 31
11 FF4 59
11 FF3 17
11 FF4 8F

Cont 4 later
Problem reported with 74L500.

Analysis: With a 74L500 the -RAS line is overloaded and the H→L transition is slow, irregular and delayed. With a 7400 it is better, 74H00 better yet. 74500 rings off, but probably due to scope.

Flokey board has power supply voltage of 4.75v.

Suggestions: Use 74S373 for the RAS address driver. This improves tuning under all circumstances.

Use 74H00 (or 74500 if the signal quality can be verified). This fixes the H→L -RAS transition.

If the RAM is slow, a 7404 instead of 74L504 will give 3ns more RAS-CAS interval. The value of this is questionable.

Use supply voltage = 5v.

Criticism: The overloaded 74L500 is an engineering error. The source of the error was either sloppy debugging or due to the prototype also using a 7400 (because 74L500's not available.

The 74S373 174L5373 is OK either way, and the original engineering used all LS.

Supply voltage is not an engineering problem.
Problem is definitely write related. Memory write foils and previous contents are still there. Where does it go??

```
    FF3    31
    FF4    57
    FF3    17
    FF4    BF
    FF2    0F
    FF4    4F
    FF7    18
```

Ram test program R3.

Designed to allow detection of a mis-write. Checks until error then calculates syndrome of memory. Syndrome will reveal if and the address of an extraneous write.

H00 -> no errors, no extra writes

LS06 -> 57A9  error

17A9 extra write

57A9  error

NO extra write

57A9  error

17 A9 extra write (2C) in 17A9 07 error

57A9  error

NO extra write
23 Oct 82

Changed to 741109

745373 - low address

Supply @ 5.0 V
RAS & CAS 20µs/div 1V/div
- RAS driver: 74LS500
RAS & CAS 20ns/div 1V/div
using 74H06, 74S373, 4.74 V supply

RAS & CAS 20ns/div 1V/div
using 74H06, 74S373, 5.00 V supply
CAS & and Aφ  20ns/div  1V/div
74144, 745378, 5V supply

CAS & Aφ  20ns/div  1V/div
741400 & 745373, 5V supply
BF1B problem:
BF1B board screws up ram accesses to addresses XFFXX.

Problem: incorrect logic on BF1B board: output drivers gated with I/O address without I/O access.

Solution:
\[ \text{ACKEN} \rightarrow \text{R2SPIC} \rightarrow \text{ACKEN} \]
\[ \text{PAREN} \rightarrow \text{INTEN} \rightarrow \text{-BDEN} \]

Added to BF1B to make BF1B2. Board changed. Untested.