# Search Detail

## Document Info

<table>
<thead>
<tr>
<th>Title:</th>
<th>Completing the Journey of Moore’s Law</th>
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<tr>
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<td>Requestor:</td>
<td>DEBENEDICTIS,ERIK P.</td>
</tr>
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<td>Submit Date:</td>
<td>05/03/2004</td>
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## Author(s)

**DEBENEDICTIS,ERIK P.**

## Event (Conference/Journal/Book) Info

<table>
<thead>
<tr>
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<th>Seminar at University of Illinois at Urbana-Champaign</th>
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## Routing Details

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In the future, please use correct funding statement. printed 5/14/2004 (al)

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For Review and Approval process questions please contact the **Application Process Owner**
Completing the Journey of Moore’s Law

Presentation at University Of Illinois
May 5, 2004

Erik P. DeBenedictis
Sandia National Laboratories
Potentials of Supercomputing

Current Machines

Irreversible Logic

Reversible Logic

Quantum Computing

Current Strategy: Follow Moore’s Law Indefinitely

This Talk

Performance

Year

2004

2016
Outline

• Applications of the Future
  • Limits of Moore’s Law
  • How to Reach the Limit
    – Aerogel model
    – Applications Modeling
  • No Need For a Breakthrough
• Architecture
• Beyond Moore’s Law
Simulation of Physics on a Computer

• Space is divided into cells, each with computer variables representing the physical state of the volume represented by the cell.
• The computer updates the state of a cell for successive time intervals $\Delta T$ based on some physical laws.
• I.e. $S_{ijk}' = f(S_{ijk}, \text{states of nearby cells})$.

Cell with “state” of space.
Fourth Power Scaling Rule

Reference

2× spatial resolution, 2× time steps $\rightarrow 2^4 \times$ FLOPS
Example: Earthquake Risk Mitigation

• In an Earthquake-prone region
  – Some areas the size of city blocks shake a lot
  – Others are stable

• This effect is due to focusing or deflection of seismic waves due to underground rock structure

• Mitigation
  – Identify dangerous areas and avoid building there
  – Identify dangerous areas by simulating many typical Earthquakes and noting the shaking
  – Requires an image of the underground rock structure
**Example Application: Earthquake Mitigation**

- **Forward simulation**
  - Match the results of a seismic simulation with observed data from seismographs

- **Imaging**
  - Deduce the structure of rock under the region (imaging) by repeatedly simulating the error from forward simulation by adjoint methods

Example: Earthquake Risk Mitigation

• Today
  – Codes run at Caltech, Pittsburgh Supercomputer
  – Uses frequencies to 1 Hz, or a wavelength or several miles in rock
  – Computers are about 5 Teraflops

• Limit
  – Seismographs collect data to 20 Hz or more, or hundreds of feet in rock
  – Buildings are hundreds of feet in size, so this is useful resolution
  – Required computer 5 Teraflops × $20^4 = 1$ Exaflops
Earthquake Risk Mitigation

- Algorithms: Written
- Code: Runs
- Input Data: Exists
- Consequence of Not Proceeding: People Die
- Required FLOPS: $1E = 1000P = 1,000,000T$
  - $25,000 \times$ Earth Simulator
Global Climate

• Objective
  – Collect data about Earth
  – Model climate into the future
  – Provide “decision support” and ability to “mitigate”

• Approaches
  – Climate models exist, but need they more resolution, better physics, and better initial conditions (observations of the Earth)

• Computer Resources Required
  – Increments over current workstation on next slide
### FLOPS Increases for Global Climate

<table>
<thead>
<tr>
<th>Issue</th>
<th>Motivation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Zetaflops</td>
<td>Ensembles, scenarios</td>
</tr>
<tr>
<td></td>
<td>10× Range of model variability</td>
</tr>
<tr>
<td>100 Exaflops</td>
<td>Run length</td>
</tr>
<tr>
<td></td>
<td>100× Long-term implications</td>
</tr>
<tr>
<td>1 Exaflops</td>
<td>New parameterizations</td>
</tr>
<tr>
<td></td>
<td>100× Upgrade to “better” science</td>
</tr>
<tr>
<td>10 Petaflops</td>
<td>Model Completeness</td>
</tr>
<tr>
<td></td>
<td>100× Add “new” science</td>
</tr>
<tr>
<td>100 Teraflops</td>
<td>Spatial Resolution</td>
</tr>
<tr>
<td></td>
<td>10^4× (10^3×-10^5×) Provide regional details</td>
</tr>
<tr>
<td>10 Gigaflops</td>
<td>Current</td>
</tr>
</tbody>
</table>

Outline

• Applications of the Future
  • Limits of Moore’s Law
  • How to Reach the Limit
    – Aerogel model
    – Applications Modeling
  • No Need For a Breakthrough
• Architecture
• Beyond Moore’s Law
### Table: Properties of Double Precision Floating Point

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<td>Estimate</td>
</tr>
<tr>
<td>1 Exaflops</td>
<td>8 Petaflops</td>
<td>Uncertainty (6×)</td>
<td>Gap in chart</td>
</tr>
<tr>
<td><strong>Assumption:</strong> Supercomputer consumes 2 MW wall power = 500 KW to chips</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Comments:
- **Estimate**
- **Expert Opinion**

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**Red Storm contract**
Thermal Noise Limit

This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function.
— R. Landauer 1961

kT “helper line,” drawn out of the reader’s focus because it wasn’t important at the time of writing
— Carver Mead, Scaling of MOS Technology, 1994
Metaphor to FM Radio on Trip to Chicago

- You drive to Chicago listening to FM radio
- Music clear for a while, but noise creeps in and then overtakes music
- Why?
  - Signal at antenna weakens
  - Thermal electron noise constant at $k_B T$

- Analogy: You live out the next dozen years buying PCs every couple years
- Electrical effect
  - Moore’s Law causes switching energy of gates to decrease at about 30% per year
  - Thermal electron noise constant at $k_B T$

FM Radio and End of Moore’s Law

Driving away from FM transmitter $\rightarrow$ less signal
Noise from electrons $\rightarrow$ no change

Increasing numbers of gates $\rightarrow$ less signal power
Noise from electrons $\rightarrow$ no change
Amount of Reliability Needed

- We expect computers to be reliable.
- A future supercomputer will perform $10^{30}$-$10^{40}$ operations in its lifetime.
- Error rate should be $< 10^{-30} - 10^{-40}$.
- Reliability due to thermal noise about $e^{-E/kt}$.
- Need about $e^{-100}$ error rate, or 100 $k_B T$ switching energy.

<table>
<thead>
<tr>
<th>SNR (db)</th>
<th>Power Ratio</th>
<th>$P_{error}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
<td>$3.9 \times 10^{-6}$</td>
</tr>
<tr>
<td>14</td>
<td>25</td>
<td>$6.8 \times 10^{-13}$</td>
</tr>
<tr>
<td>18</td>
<td>63</td>
<td>$1.4 \times 10^{-29}$</td>
</tr>
<tr>
<td>22</td>
<td>160</td>
<td>$3.3 \times 10^{-71}$</td>
</tr>
<tr>
<td>26</td>
<td>400</td>
<td>$1.8 \times 10^{-175}$</td>
</tr>
<tr>
<td>30</td>
<td>1,000</td>
<td>$4.5 \times 10^{-437}$</td>
</tr>
<tr>
<td>34</td>
<td>2,500</td>
<td>$7.1 \times 10^{-1094}$</td>
</tr>
<tr>
<td>38</td>
<td>6,300</td>
<td>$2.2 \times 10^{-2743}$</td>
</tr>
<tr>
<td>42</td>
<td>16,000</td>
<td>$1.8 \times 10^{-6886}$</td>
</tr>
<tr>
<td>46</td>
<td>40,000</td>
<td>$3.8 \times 10^{-17293}$</td>
</tr>
<tr>
<td>50</td>
<td>100,000</td>
<td>$3.2 \times 10^{-43433}$</td>
</tr>
<tr>
<td>54</td>
<td>250,000</td>
<td>$8.1 \times 10^{-10194}$</td>
</tr>
<tr>
<td>58</td>
<td>630,000</td>
<td>$1.8 \times 10^{-274025}$</td>
</tr>
<tr>
<td>62</td>
<td>1,500,000</td>
<td>$9.6 \times 10^{-688315}$</td>
</tr>
</tbody>
</table>

\[ q := \int e^{-\frac{x^2}{2}} \, dx \rightarrow \sqrt{2 \pi} \times 10^{\frac{m_e}{10}} \]
Noise Levels

- 0 db Limit of hearing
- 20 db Rustling leaves
- 40-50 db Typical neighborhood
- 60-70 db Normal conversation
- 80 db Telephone dial tone
- 85 db City traffic inside car
- 90 db Train whistle @500’
- 95 db Subway train @200’
- 90-95 db Ear damage

- Today: 50 db
  - Thermal noise: Logic:: Rustling leaves: Talking
- 2016: 30 db
  - Thermal noise: Logic:: Talking: Train Whistle
- Reliability limit 20 db
  - Thermal noise: Logic:: Outside neighborhood: Talking
Personal Observational Evidence

• Have radios become better able to receive distant stations over the last few decades with a rate of improvement similar to Moore’s Law?

• You judge from your experience, but the answer should be that they have not.

• Therefore, electrical noise does not scale with Moore’s Law.
SIA Semiconductor Roadmap

• Generalization of Moore’s Law
  – Projects many parameters
  – Years through 2016
  – Includes justification
  – Panel of experts
    • known to be wrong
  – Size between Albuquerque white and yellow pages

International Technology Roadmap for Semiconductors (ITRS), see http://public.itrs.net
Semiconductor Roadmap

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2010</th>
<th>2013</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Pitch (nm)</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>MPU / ARB Pitch (nm)</td>
<td>20</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm)</td>
<td>90</td>
<td>80</td>
<td>70</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>80</td>
<td>80</td>
<td>70</td>
</tr>
<tr>
<td>Physical gate length high-performance (HP) (nm)</td>
<td>10</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>Equivalent physical oxide thickness for high-performance $T_{ox}$ (EOT) (nm)</td>
<td>0.5</td>
<td>0.4</td>
<td>0.6</td>
</tr>
<tr>
<td>$T_{ox}$ electrical equivalent (nm)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Nominal power supply voltage ($V_{dd}$) (V)</td>
<td>1.2</td>
<td>1.0</td>
<td>0.9</td>
</tr>
<tr>
<td>Nominal high-performance NMOS sub threshold leakage current, $I_{dsat}$ (at 25°C) (mA/m)</td>
<td>3</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Nominal high-performance NMOS saturation drive current, $I_{dsat}$ (at $V_{dd}$ at 25°C) (mA/m)</td>
<td>1200</td>
<td>1500</td>
<td>1500</td>
</tr>
<tr>
<td>Required percent current-drive “mobility/transconductance improvement” (%)</td>
<td>30%</td>
<td>70%</td>
<td>100%</td>
</tr>
<tr>
<td>Saturation source/drain resistance (Rsd) (ohm-mil)</td>
<td>110</td>
<td>90</td>
<td>80</td>
</tr>
<tr>
<td>Saturation source/drain resistance (Rsd) percent</td>
<td>25%</td>
<td>30%</td>
<td>35%</td>
</tr>
<tr>
<td>Saturation capacitance percent of ideal gate</td>
<td>31%</td>
<td>36%</td>
<td>42%</td>
</tr>
<tr>
<td>High-performance NMOS device $t_{ox}$ (ps)</td>
<td>0.39</td>
<td>0.22</td>
<td>0.15</td>
</tr>
<tr>
<td>Relative device performance</td>
<td>11.3</td>
<td>7.2</td>
<td>10.7</td>
</tr>
<tr>
<td>Energy per (W/μm²–3) device switching transition ($C_{gate}$ ($V_{dd}$+8 V) (W/Device)</td>
<td>0.015</td>
<td>0.007</td>
<td>0.002</td>
</tr>
<tr>
<td>Static power dissipation per (W/μm²–3) device (White/Device)</td>
<td>9.7E-08</td>
<td>1.4E-07</td>
<td>1.1E-07</td>
</tr>
</tbody>
</table>

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known
# Limits for a Red Storm-Sized Computer

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<td>Gap in chart</td>
</tr>
<tr>
<td>1 Exaflops</td>
<td>8 Petaflops</td>
<td>Improved devices (4×)</td>
<td>Estimate</td>
</tr>
<tr>
<td>Assumption: Supercomputer consumes 2 MW wall power = 500 KW to chips</td>
<td>80 Teraflops</td>
<td>Projected ITRS improvement to 22 nm (100×)</td>
<td>ITRS committee of experts</td>
</tr>
<tr>
<td></td>
<td>40 Teraflops</td>
<td>Lower supply voltage (2×)ITRS committee of experts</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Red Storm contract</td>
<td></td>
</tr>
</tbody>
</table>

**Table Notes:**
- **Assumption:** Supercomputer consumes 2 MW wall power = 500 KW to chips
- **Estimate:**
  - 25 Exaflops 200 Petaflops
  - 4 Exaflops 32 Petaflops
  - 1 Exaflops 8 Petaflops
- **Uncertainty:** (6×)
- **Gap in chart:**
- **Estimation:**
  - Projected ITRS improvement to 22 nm (100×)
  - Lower supply voltage (2×)
Outline

• Applications of the Future
• Limits of Moore’s Law
  • How to Reach the Limit
    – Aerogel model
    – Applications Modeling
• No Need For a Breakthrough
• Architecture
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Can We Reach the Limit?

• Method: Compare modeled running time on perfect computer to real computer
• Application: Local calculations with global time step (SOR)
• Technology comparison:
  – 22 nm transistors with 3D atom-by-atom assembly
  – Our best shot at an architecture
• Definition of Success: Our best shot comes within a constant factor of the theoretical peak
Aerogel Computer

• Devise algorithm for a hypothetical aerogel computer
  – Cell may be gate
  – Cell may be memory
  – Is space for cooling, but no cooling
• Model application runtime
• Engineer real computer
• Model application runtime
• If runtimes similar, you succeeded

Element = Bit of memory or part of logic gate (transistor)
Aerogel Cooling

- Inflate aerogel computer to point where heat emerging from faces is less than capacity of a designated cooling system
  - Air 45KW/m²
  - Water 62MW/m²
  - Pulse $\infty$W/m²
Architecture Target

ALU/FPU that Evaluates Laws of Physics at Max Efficiency:
Signal Processor

Cell State Storage for K Cells With Max Efficiency Access for Only The Needed Access Pattern

Neighbors in Mesh
Global Synchronization

- Gather Dimension 1
- Gather Dimension 2
- Gather Dimension 3

Termination Decision & SOR Control (HOST)
Application Modeling

• Sample Problem
  – 3D finite difference equation with global synchronization
  – SOR method

\[ T_{\text{Step}} = \frac{K \times F_{\text{cell}}}{\text{flop rate}} + T_{\text{Global}} \]

– where
  • \( K \) is memory size

• Global synchronization limited by speed of light

\[ T_{\text{Global}} \geq \frac{2 \sqrt{3} \times L_{\text{Edge}}}{c} \]

– where
  • \( L_{\text{Edge}} \) is edge dimension of cube

\[ 6 \times L_{\text{Edge}}^2 \times C_x \leq \text{Power} \]
Actual Applications Modeling

- Actual code was several hundred lines of C++
- Theoretical limit covered
  - Coolant
- Realistic covered
  - Layout on a 2D surface of a particular size
  - Heat sink limits
  - I/O bandwidth from chip
  - Coolant
Performance on Sample Problem

Interpretation:
- There is a limit, but it is not in the range of concern
- Better cooling yields higher limit, but mostly out of the range of our concern

Legend:
- Air Cooling
- Water Cooling
- Fractal Plumbing
- Pulse (no cooling)
- Thick=Realistic
- Thin=Theoretical Limit
Cost Efficiency

Plotting TFLOPS/Operating Cost of 15¢/KWH (electric power) + $1000/chip (capital cost) + $12/ft²/year (machine room space)

Legend:
- Air Cooling
- Water Cooling
- Fractal Plumbing
- Pulse (no cooling)

*Thick=*Realistic
*Thin=*Theoretical Limit

Water cooling is better – but not by much!
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Example of Computer at Physics Limit

- Sandia is often approached by people who say we need some elaborate technology in order to run our applications at the Petaflops level
  - Do we need elaborate technology?
  - Is the person just looking for research funding?
- Question: can we make a computer that runs at the limits out of inexpensive components?
  - Yes, subsequent slides are example
Design minimizes signal travel distance while maximizing use of surface area for cooling.
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- How to Reach the Limit
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Which Microarchitecture?

• Task: Pick a winner
  – Candidates μP, PIM, vector, FPGA, reconfigurable, streaming, maybe more
  – Each has advantages
  – Not clear which is best
  – Government gets bad press for picking winners too early

• Why do we pick winners
  – Logic is a scarce resource
  – But hang on a minute, don’t we have more transistors than we know what to do with, and even turn some off at times?

• Can we change the rules of the game to make NOT picking a winner a virtue?
Multi-Architecture Idea

• Architecture to comprise
  – μP and accelerator architectures 1 and 2
  – Power control circuit so only one is turned on at a time

• Benefit
  – Can expect support from cluster community and advocates of architectures 2 and 3

• Arch2=Vector, Arch3=PIM?
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Beyond Moore’s Law

Circuits & Logic Families

- Reversible: \( E \geq 0 \)
- Adiabatic: Irreversible \( E \geq k_B T \log_e 2 \)
- Dissipative: Irreversible \( E \geq 100 k_B T \)

Transistors

- Class: Floating Point, Logic, Analog
- e.g. “Rod Logic”
- e.g. “Helical Logic”

Next Slides

Performance

Devices with Better Figure of Merit

Sandia National Laboratories
Reversible Logic

• Reversible logic dissipates energy through “friction”
• If you run reversible logic at speed \( \propto 1/n \), it will dissipate power \( \propto 1/n^2 \)
• However, any design will have a parasitic power loss, so actual loss is not \( \propto 1/n^2 \), but
  \[
  \text{Power} = \frac{P_0}{n^2} + P_{\text{parasitic}}
  \]
• Measured power down \( 4 \times \), limit \( 2000 \times \)
Reversible Multiplier Status

- 8×8 Multiplier Designed, Fabricated, and Tested by IBM & University of Michigan
- Power savings was up to 4:1
Reversible Microprocessor Status

• Status
  – Subject of Ph. D. thesis
  – Chip laid out (no floating point)
  – RISC instruction set
  – C-like language
  – Compiler
  – Demonstrated on a PDE
  – However: really weird and not general to program with +=, -=, etc. rather than =
Thought Model for Reversible Red Storm

- Replace each Red Storm node with chips constructed from $n^2 \approx 1000$ layers of reversible logic operating $1/n \approx 1/30$ speed
- Overall system $30 \times$ faster, same power, $1000 \times$ nodes

• Will become feasible for small “line width”
<table>
<thead>
<tr>
<th></th>
<th>Conventional Logic Red Storm</th>
<th>Reversible n=30 Red Storm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nodes</td>
<td>10,000</td>
<td>10,000,000</td>
</tr>
<tr>
<td>FLOPS/node</td>
<td>4 Gigaflops</td>
<td>100 Megaflops</td>
</tr>
<tr>
<td>Total FLOPS</td>
<td>40 Teraflops</td>
<td>1 Petaflops</td>
</tr>
</tbody>
</table>
Summary

• Applications based on “simulating physics on a computer” scale up quite a ways
  – Gave one example at 1 Exaflops & 1 Zetaflops
• Semiconductor roadmap comes pretty close to physical limits for current class of computers
  – Had chart with numerical FLOPS targets
  – Microprocessors cost about 100×
• Other classes of computers are possible, but introduce disruptive change
Ideas for Future Work

• For computer architecture and software
  – Show scalability to the physical limits, but not beyond

• Estimate FLOPS for important problems to society that can be solved with computers
  – Which will be solvable with a computer of the current class, but scaled by Moore’s Law?
  – Which will require a new class of computer?
    • These problems create a mandate for research into new classes of computer
Backup
## General Specifications at Physics Limit

<table>
<thead>
<tr>
<th></th>
<th>Red Storm</th>
<th>Limit µP Mode</th>
<th>Limit Turbo Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nodes</td>
<td>10,000</td>
<td>200,000</td>
<td>2,000,000</td>
</tr>
<tr>
<td>Node Type</td>
<td>µP</td>
<td>µP</td>
<td>TBD – say 10 vector pipes</td>
</tr>
<tr>
<td>Clock</td>
<td>2 GHz</td>
<td>20 GHz</td>
<td>20 GHz</td>
</tr>
<tr>
<td>Flops/node</td>
<td>4 GFLOPS</td>
<td>40 GFLOPS</td>
<td>400 GFLOPS</td>
</tr>
<tr>
<td>Sys. Peak</td>
<td>40 TFLOPS</td>
<td>8 PFLOPS</td>
<td>800 PFLOPS</td>
</tr>
<tr>
<td>MPI Latency</td>
<td>2.5 µS</td>
<td>100 ns</td>
<td>N/A – no MPI</td>
</tr>
<tr>
<td>Power</td>
<td>2 MW</td>
<td>2 MW</td>
<td>2 MW</td>
</tr>
</tbody>
</table>
The Cost of Beating Moore’s Law

• A “1” and “0” must have more than $100\times$ the thermal energy to avoid errors
  – Lowering the temperature doesn’t help, it just shifts power to the refrigerator

• Today’s irreversible logic destroys “1”s and “0”s at each gate. However, “reversible computing” recycles the energy in “1”s and “0”s. There is no known limit to “reversible computing.”

• Quantum computing offers the possibility of exponential speedups
Packaging for a Spatial Locality

• Basic Module
  – 2 Nodes
  – Each node is an ASIC System On Chip Processor In Memory
  – Each node has memory under ASIC
  – Each module includes a power module
  – Six mesh Interconnects

• Modules connect end-to-end in “Shish Kabobs”
Packaging for a Spatial Locality

- Entire supercomputer is a single structure
- All mesh network wires are of constant length (8” max)
- Air flows front to back
  - General approach will work for liquid cooling as well
Nearest-Neighbor Interconnect

- **X Dimension**
  - From one board to another laying in the same plane – 2”
- **Y Dimension**
  - 8” from one board to another spaced above or below – 8”
- **Z Dimension**
  - Along the Shish Kabob – 4”
  - Name courtesy Monty Denneau IBM
Maintenance

• Each “Shish Kabob” can be removed for maintenance
• Connects via side-connect technology
  – Similar to Cray shuttle connectors on T3E and X1
• Each Shish Kabob can be composed of segments to avoid limits on PC board technology
• Depth should be OK to 6’
Backup: Landauer’s Arguments

• Landauer makes three arguments in his 1961 paper
  – Kinetetics of a bistable well
  – Entropy generation
• We review the second →

• Entropy of a system in statistical mechanics:
  \[ S = k_B \log_e(W) \]
  \( W \) is number of states
• Entropy of a mechanical system containing a flip flop in an unknown state:
  \[ S = k_B \log_e(2W) \]
• After clearing the flip flop:
  \[ S = k_B \log_e(W) \]
• Difference \( k_B \log_e(2) \)
• Second law of thermodynamics says entropy of universe must increase
  – Entropy is disorder
• Say you clear a computer memory of n bits. The computer’s memory is initially disordered (arbitrary bits) but becomes ordered (all zero). Entropy goes down.
• However, entropy of universe must increase.
• Resolution is that the material of the memory chip becomes more disordered (hotter), offsetting the information in the memory
• A logic gate with multiple inputs but one output has fewer output states than input states: same idea
This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of $kT$ for each irreversible function.
– R. Landauer 1961

$kT$ “helper line,” drawn out of the reader’s focus because it wasn’t important at the time of writing
– Carver Mead, Scaling of MOS Technology, 1994
A floating point unit has about 100,000 gates.

About 20,000 gates will switch for each operation.

Therefore,

\[ E_{\text{FLOP}} \approx 20,000 \times E_{\text{gate}} \approx 2,000,000 \times k_B \times T \]

Landauer limit is:

100 TFLOPS/watt

Accounting for engineering losses, more realistic:

10 TFLOPS/watt

If a \(\mu\)P is 1% efficient, the probable limit for a microprocessor is:

10 TFLOPS/watt chip
Backup: What About Cryogenics?

• Minimum power per logic op $100 \, k_B T$
• Minimum power per FLOP $2 \times 10^6 \, k_B T$
• Analysis
  – At any $T$, performance may depend on cooling
  – Cutting $T$ won’t save power because of offsetting power in refrigerator, but may make cooling system more efficient
• However
  – Applications modeling indicates DOE apps aren’t especially dependent on cooling
• Conclusion: Use room temperature
Backup: Authority on μP Efficiency

Data parallelism realizes full potential of increased transistor count

Citation:
Bill Dally,
ASCI PI
Meeting 2004
Backup: Authority on μP Efficiency

Data parallelism realizes full potential of increased transistor count

Citation:
Bill Dally,
ASCI PI
Meeting 2004

2004: 125:1
Backup: Languages

• For many years, computer languages have targeted higher programmer productivity, trading easy programming for higher resource consumption during execution. This was believed to be OK because Moore’s Law would cut the excess cost over time. Not so anymore.

• Need to study languages for mature “irreversible logic” computers that are both easy to use and avoid excessive use of resources.
Backup Slide: Analog Computing

- **Floating Point Energy/Op**
  - $20,000 \times 100 \times k_B T = 2 \times 10^6 k_B T$

- **Analog Energy/Op**
  - $k_B T \log_e(\# \text{ states})$
  - $k_B T \log_e(2^{64})$
  - $64 k_B T \log_e 2$
  - $44 k_B T$

- **Analog 45,000 more efficient**

- **Heisenberg Uncertainty Principle**
  - $\Delta E \Delta t \geq \hbar/(2\pi)$

- **Waiting Time**
  - $\Delta E = 2^{-64} \times 64 k_B T \log_e 2$
  - $\Delta t \geq \frac{\hbar}{2\pi \times 2^{-64} \times 64 k_B T \log_e 2}$
  - $\Delta t \geq \sim 3 \text{ hours}$

- **Analog really slow**