### Document Info

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<td>Document Number</td>
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<td>SAND Number</td>
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<td>Sandia Contact</td>
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<td>DEBENEDICTIS, ERIK P.</td>
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<tr>
<td>Peer Reviewed?</td>
<td>N</td>
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### Event (Conference/Journal/Book) Info

| Name                  | Computing Frontiers 2005             |
| City                  | Ischia                              |
| State                 |                                     |
| Country               | Italy                               |
| Start Date            | 05/04/2005                          |
| End Date              | 05/06/2005                          |

### Partnership Info

| Partnership Involved | No                                    |
| Agreement Number     |                                       |

### Patent Info

| Scientific or Technical in Content | Yes |
| Technical Advance               | No  |
| TA Form Filed                   | No  |
| SD Number                       |     |

### Classification and Sensitivity Info

| Title                        | Unclassified-Unlimited              |
| Abstract                     | Document: Unclassified-Unlimited    |
| Additional Limited Release Info | None.                              |
| DUSA                         | None.                               |
|                             |                                      |

### Routing Details

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<td>SUMMERS, RANDALL M.</td>
<td>SUMMERS, RANDALL M.</td>
<td>04/22/2005</td>
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<td>KRAMER, SAMUEL</td>
<td>06/05/2007</td>
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For Review and Approval process questions please contact the **Application Process Owner**
Reversible Logic for Supercomputing

*Presented at RC’05:*
*The First Int’l. Workshop on Reversible Computing*

**Erik P. DeBenedictis**
Sandia National Laboratories

May 5, 2005
Applications and $100M$ Supercomputers

<table>
<thead>
<tr>
<th>System Performance</th>
<th>Applications</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Zettaflops</td>
<td>Full Global Climate [Malone 03]</td>
<td>③ Nanotech + Reversible Logic (green) best-case logic (red)</td>
</tr>
<tr>
<td>100 Exaflops</td>
<td>Compute as fast as the engineer can think [NASA 99]</td>
<td>② Architecture: IBM Cyclops, FPGA, PIM</td>
</tr>
<tr>
<td>10 Exaflops</td>
<td>100× 1000× [SCaLeS 03]</td>
<td>① Red Storm/Cluster</td>
</tr>
<tr>
<td>1 Exaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 Teraflops</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Objectives and Challenges

• Could reversible computing have a role in solving important problems?
  – Maybe, because power is a limiting factor for computers and reversible logic cuts power
• However, a complete computer system is more than “low power”
  – Processing, memory, communication in right balance for application
  – Speed must match user’s impatience
  – Must use a real device, not just an abstract reversible device
Outline

• An Exemplary Zettaflops Problem
• The Limits of Current Technology
• Arbitrary Architectures for the Current Problem
  – Searching the Architecture Space
  – Bending the Rules to Find Something
  – Exemplary Solution
• Conclusions
“Simulations of the response to natural forcings alone … do not explain the warming in the second half of the century”

“…model estimates that take into account both greenhouse gases and sulphate aerosols are consistent with observations over this period” - IPCC 2001

Stott et al, Science 2000
## FLOPS Increases for Global Climate

<table>
<thead>
<tr>
<th>Issue</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ensembles, scenarios</td>
<td>Embarrassingly Parallel</td>
</tr>
<tr>
<td>Run length</td>
<td>Longer Running Time</td>
</tr>
<tr>
<td>New parameterizations</td>
<td>More Complex Physics</td>
</tr>
<tr>
<td>Model Completeness</td>
<td>More Complex Physics</td>
</tr>
<tr>
<td>Spatial Resolution</td>
<td>Resolution</td>
</tr>
<tr>
<td>Clusters Now In Use</td>
<td>(100 nodes, 5% efficient)</td>
</tr>
</tbody>
</table>

Outline

• An Exemplary Zettaflops Problem
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• Conclusions
### Table

<table>
<thead>
<tr>
<th>Expert Opinion</th>
<th>Best-Case Logic</th>
<th>Microprocessor Architecture</th>
<th>Physical Factor</th>
<th>Source of Authority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimate</td>
<td>100 Exaflops</td>
<td>800 Petaflops</td>
<td>Reliability limit</td>
<td>Esteemed physicists</td>
</tr>
<tr>
<td></td>
<td>25 Exaflops</td>
<td>200 Petaflops</td>
<td>Derate 20,000 convert</td>
<td>Floating point engineering</td>
</tr>
<tr>
<td></td>
<td>4 Exaflops</td>
<td>32 Petaflops</td>
<td></td>
<td>Estimate</td>
</tr>
<tr>
<td></td>
<td>1 Exaflops</td>
<td>8 Petaflops</td>
<td></td>
<td>Gap in chart</td>
</tr>
<tr>
<td></td>
<td>100 Exaflops</td>
<td>800 Petaflops</td>
<td>Improved devices</td>
<td>Estimate</td>
</tr>
<tr>
<td></td>
<td>25 Exaflops</td>
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<td></td>
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</tr>
<tr>
<td></td>
<td>1 Exaflops</td>
<td>8 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assumption: Supercomputer is size &amp; cost of Red Storm: US$100M budget; consumes 2 MW wall power; 750 KW to active components</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Notes
- **2×10^{24}** logic ops/s
- **Reliability limit 750KW/(80k_B T)**
- Derate 20,000 convert logic ops to floating point
- Floating point engineering (64 bit precision)
- Derate for manufacturing margin (4×)
- Estimate
- Uncertainty (6×)
- Gap in chart
- Improved devices (4×)
- Estimate
- Projected ITRS improvement to 22 nm (100×)
- ITRS committee of experts
- Lower supply voltage (2×)
- ITRS committee of experts
- Red Storm contract
Metaphor: FM Radio on Trip to in USA

- You drive to a distant listening to FM radio
- Music clear for a while, but noise creeps in and then overtakes music

Analogy: You live out the next dozen years buying PCs every couple years

- PCs keep getting faster
  - clock rate increases
  - fan gets bigger
  - won’t go on forever

Why…see next slide

FM Radio and End of Moore’s Law

- Driving away from FM transmitter → less signal
- Noise from electrons → no change

- Increasing numbers of gates → less signal power
- Noise from electrons → no change
# Scientific Supercomputer Limits

<table>
<thead>
<tr>
<th>Best-Case Logic</th>
<th>Microprocessor Architecture</th>
<th>Physical Factor</th>
<th>Source of Authority</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 Exaflops</td>
<td>800 Petaflops</td>
<td>Reliability limit</td>
<td>Esteemed physicists</td>
</tr>
<tr>
<td>80 Teraflops</td>
<td></td>
<td>750KW/(80k_B T) (T=60°C junction temperature)</td>
<td></td>
</tr>
<tr>
<td>Estimate</td>
<td>25 Exaflops</td>
<td>Derate 20,000 convert logic ops to floating point</td>
<td>Floating point engineering (64 bit precision)</td>
</tr>
<tr>
<td></td>
<td>200 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4 Exaflops</td>
<td>Derate for manufacturing margin (4×)</td>
<td>Estimate</td>
</tr>
<tr>
<td></td>
<td>32 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assumption:</td>
<td>1 Exaflops</td>
<td>Uncertainty (6×)</td>
<td>Gap in chart</td>
</tr>
<tr>
<td>Supercomputer</td>
<td>8 Petaflops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>is size &amp; cost</td>
<td>80 Teraflops</td>
<td>Improved devices (4×)</td>
<td>Estimate</td>
</tr>
<tr>
<td>of Red Storm:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>US$100M budget;</td>
<td></td>
<td>Projected ITRS</td>
<td>ITRS committee of experts</td>
</tr>
<tr>
<td>consumes 2 MW</td>
<td></td>
<td>improvement to 22 nm</td>
<td></td>
</tr>
<tr>
<td>wall power; 750</td>
<td></td>
<td>(100×)</td>
<td></td>
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<tr>
<td>KW to active</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>components</td>
<td></td>
<td>Lower supply voltage (2×)</td>
<td>ITRS committee of experts</td>
</tr>
<tr>
<td>40 Teraflops</td>
<td></td>
<td>Red Storm</td>
<td>contract</td>
</tr>
</tbody>
</table>

- 2×10^{24} logic ops/s

---

**Estimate of Supercomputer: 125:1**
Outline

• An Exemplary Zettaflops Problem
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  – Exemplary Solution
• Conclusions
Supercomputer Expert System

Application/Algorithm run time model as in applications modeling

Logic & Memory Technology design rules and performance parameters for various technologies (CMOS, Quantum Dots, C Nano-tubes …)

Interconnect Speed, power, pin count, etc.

Physical Cooling, packaging, etc.

Expert System & Optimizer (looks for best 3D mesh of generalized MPI connected nodes, μP and other)

Time Trend Lithography as a function of years into the future

Results
1. Block diagram picture of optimal system (model)
2. Report of FLOPS count as a function of years into the future
Sample Analytical Runtime Model

- Simple case: finite difference equation
- Each node holds $n \times n \times n$ grid points

Volume-area rule
- Computing $\propto n^3$
- Communications $\propto n^2$

$$T_{step} = 6n^2 C_{bytes} T_{byte} + n^3 F_{grind/floprate}$$

Face-to-face
- $n^2$ cells
Expert System for Future Supercomputers

- Applications Modeling
  - Runtime
    \[ T_{\text{run}} = f_1(n, \text{design}) \]
- Technology Roadmap
  - Gate speed = \( f_2(\text{year}) \),
  - chip density = \( f_3(\text{year}) \),
  - cost = $$(n, \text{design})$$, …
- Scaling Objective Function
  - I have \( C_1 \) & can wait
    \[ T_{\text{run}} = C_2 \text{ seconds}. \]
    What is the biggest \( n \) I can solve in year \( Y \)?

- Use “Expert System” To Calculate:
  \[ \text{Max} \quad n: \$< C_1, \ T_{\text{run}} < C_2 \]
  All designs

- Report:
  \[ T_{\text{run}}(n, \text{design}) \]
  Floating operations
  and illustrate “design”
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The Big Issue

- Initially, didn’t meet constraints

Scaled Climate Model
- 2D → 3D mesh, one cell per processor

Parallelize cloud-resolving model and ensembles

One Barely Plausible Solution

Consider special purpose logic with fast logic and low-power memory

Consider only highest performance published nanotech device QDCA

Initial reversible nanotech

More Parallelism

More Device Speed
## ITRS Device Review 2016 + QDCA

<table>
<thead>
<tr>
<th>Technology</th>
<th>Speed (min-max)</th>
<th>Dimension (min-max)</th>
<th>Energy per gate-op</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>30 ps-1 µs</td>
<td>8 nm-5 µm</td>
<td>4 aJ</td>
<td></td>
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<tr>
<td>RSFQ</td>
<td>1 ps-50 ps</td>
<td>300 nm-1µm</td>
<td>2 aJ</td>
<td>Larger</td>
</tr>
<tr>
<td>Molecular</td>
<td>10 ns-1 ms</td>
<td>1 nm-5 nm</td>
<td>10 zJ</td>
<td>Slower</td>
</tr>
<tr>
<td>Plastic</td>
<td>100 µs-1 ms</td>
<td>100 µm-1 mm</td>
<td>4 aJ</td>
<td>Larger+Slower</td>
</tr>
<tr>
<td>Optical</td>
<td>100 as-1 ps</td>
<td>200 nm-2 µm</td>
<td>1 pJ</td>
<td>Larger+Hotter</td>
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<tr>
<td>NEMS</td>
<td>100 ns-1 ms</td>
<td>10-100 nm</td>
<td>1 zJ</td>
<td>Slower+Larger</td>
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<tr>
<td>Biological</td>
<td>100 fs-100 µs</td>
<td>6-50 µm</td>
<td>0.3 yJ</td>
<td>Slower+Larger</td>
</tr>
<tr>
<td>Quantum</td>
<td>100 as-1 fs</td>
<td>10-100 nm</td>
<td>1 zJ</td>
<td>Larger</td>
</tr>
<tr>
<td>QDCA</td>
<td>100 fs-10 ps</td>
<td>1-10 nm</td>
<td>1 yJ</td>
<td>Smaller, faster, cooler</td>
</tr>
</tbody>
</table>

Data from ITRS ERD Section, data from Notre Dame
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An Exemplary Device: Quantum Dots

- Pairs of molecules create a memory cell or a logic gate

Ref. “Clocked Molecular Quantum-Dot Cellular Automata,” Craig S. Lent and Beth Isaksen
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003
1 Zettaflops Scientific Supercomputer

- How could we increase "Red Storm" from 40 Teraflops to 1 Zettaflops?
- Answer
  - >2.5×10^7 power reduction per operation
  - Faster devices × more parallelism >2.5×10^7
  - Smaller devices to fit existing packaging

Not Specifically Advocating Quantum Dots

- A number of post-transistor devices have been proposed.
- The shape of the performance curves have been validated by a consensus of reputable physicists.
- However, validity of any data point can be questioned.
- Cross-checking appropriate; see →

QCA Microprocessor Status

• M. Niemier Ph. D. Thesis, University of Notre Dame
• 12 Bit µP
• CAD design tool principles
  – $10 \times$ circuit density of CMOS at same $\lambda$
• Applies to various devices
  – Metal dot 4.2 nm$^2$
  – Molecular 1.1 nm$^2$

Figure 4.6. A 2-bit QCA Simple 12 ALU with registers
Reversible Microprocessor Status

- Status
  - Subject of Ph. D. thesis
  - Chip laid out (no floating point)
  - RISC instruction set
  - C-like language
  - Compiler
  - Demonstrated on a PDE
  - However: really weird and not general to program with +=, -=, etc. rather than =
• Leading Thoughts
  – Implement CPU logic using reversible logic
    • High efficiency for the component doing the most logic
  – Implement state and memory using conventional logic
    • Low efficiency, but not many operations
  – Permits programming much like today
Supercomputer is 211K chips, each with 70.7K nodes of 5.77K cells of 240 bytes; solves 86T=44.1Kx44.1Kx44.1K cell problem. System dissipates 332KW from the faces of a cube 1.53m on a side, for a power density of 47.3KW/m². Power: 332KW active components; 1.33MW refrigeration; 3.32MW wall power; 6.65MW from power company. System has been inflated by 2.57 over minimum size to provide enough surface area to avoid overheating. Chips are at 99.22% full, comprised of 7.07G logic, 101M memory decoder, and 6.44T memory transistors. Gate cell edge is 34.4nm (logic) 34.4nm (decoder); memory cell edge is 4.5nm (memory). Compute power is 768 EFLOPS, completing an iteration in 224μs and a run in 9.88s.
Performance Curve

- Custom QDCA
- Rev. Logic
- Custom
- Rev. Logic Microprocessor
- Cluster
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Conclusions

• There are important applications that are believed to exceed the limits of irreversible logic
  – At US$100M budget
  – E. g. solution to global warming

• Reversible logic & nanotech point in the right direction
  – Low power

• Device Requirements
  – Push speed of light limit
  – Substantially sub-$k_B T$
  – Molecular scales

• Software and Algorithms
  – Must be much more parallel than today

• With all this, just barely works

• Conclusions appear to apply generally