

Cryogenic Adiabatic Transistor Circuits (CATCs)

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Overview

- Thanks to Mike Frank for inventing 2LAL circa 2000
- Quantum computer scale up creates a new demand for cold, scalable electronics
- Driver: Cryo adiabatic transistor circuits
 - Eject waste energy to room temperature electrically
- Applies to quantum computer control
 - Provides a memory to complement JJs
 - Narrow applicability; won't apply to Exascale
 - Applies to transmons, quantum dot, ion traps
 - Should work at 4 K today; will it work at mK?

Competitive research

- Paper (TAS early access)

Design and demonstration of an adiabatic-quantum-flux-parametron field-programmable gate array using Josephson-CMOS hybrid memories

Yukihiro Okuma, Naoki Takeuchi, Yuki Yamanashi, *Member, IEEE* and Nobuyuki Yoshikawa, *Senior Member, IEEE*

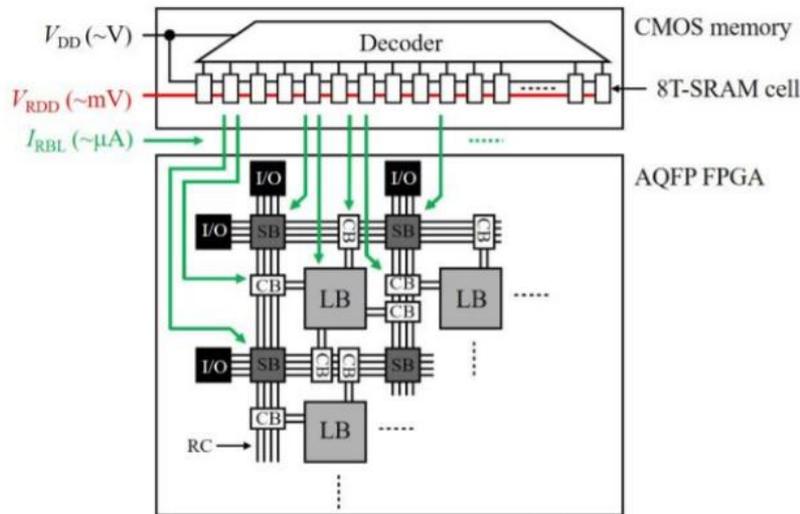


Fig. 1 Conceptual diagram of an AQFP-CMOS hybrid FPGA using a Josephson-CMOS hybrid memory.

- This approach 30,000× more efficient for trans

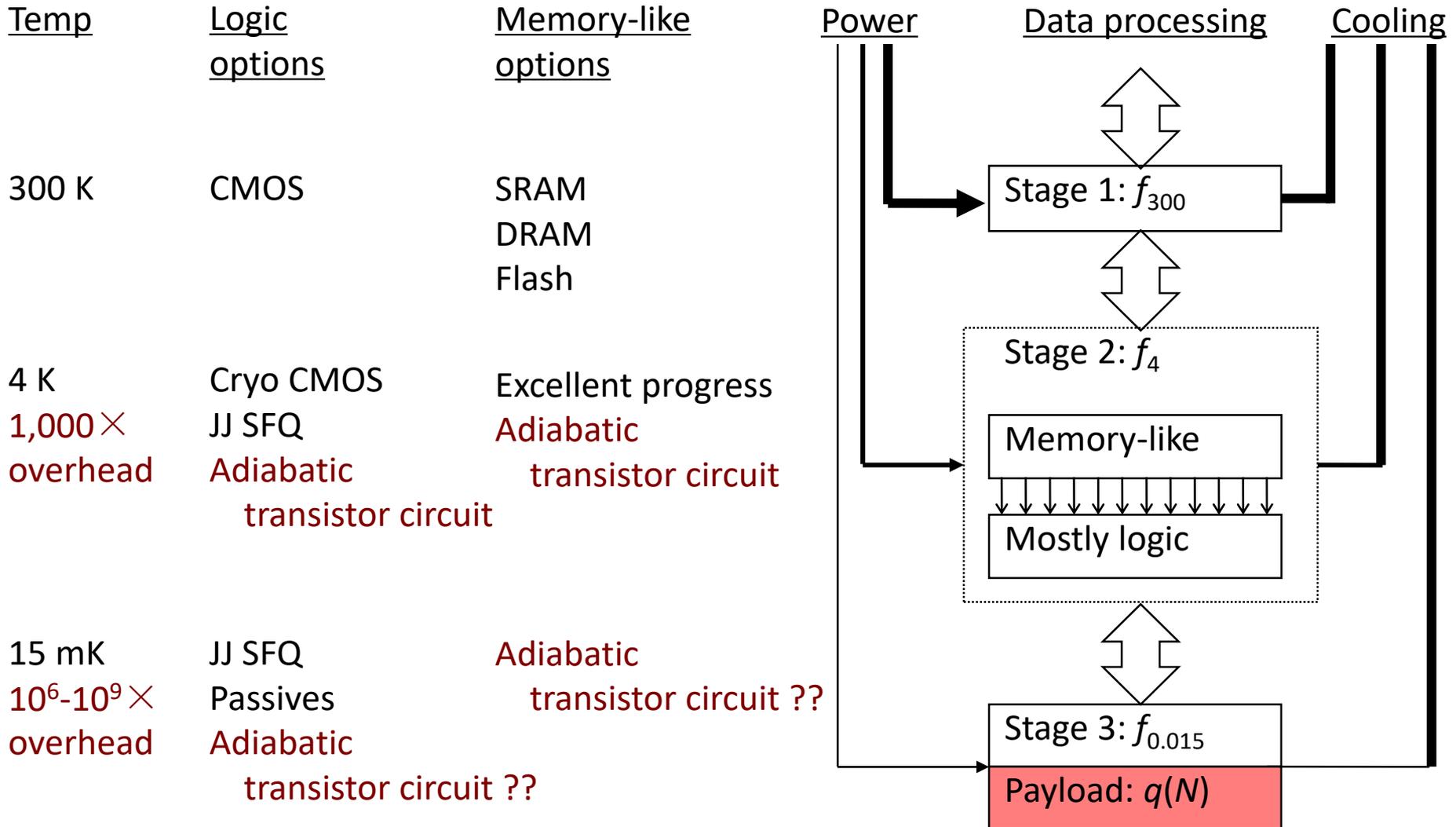
TABLE II

Junction number, circuit area, memory cell number, power consumption of AQFP-CMOS hybrid FPGAs with two-by-two and 32-by-32 logic cells.

	2×2 logic cell system	32×32 logic cell system
Junction number of AQFP FPGA circuits	1680	313220
Area of AQFP FPGA circuits [μm^2]	1960×3350	36085×44600
Number of CMOS memory cells	68	12548
Power consumption of AQFP FPGA circuits [nW]	12.4	2348
Power consumption of CMOS memories [μW]	1.02	188

	JJ	Transistor
Devices	313,220	75,288
Power	2.35E-06	1.88E-04
Power/Dev	7.50E-12	2.50E-09
Power Ratio	1.00	333.11
CATC-JJ	100	1
Advantage	33,311	

Scalable $(f_{300} \circ f_4 \circ f_{0.015} \circ q)(N)$

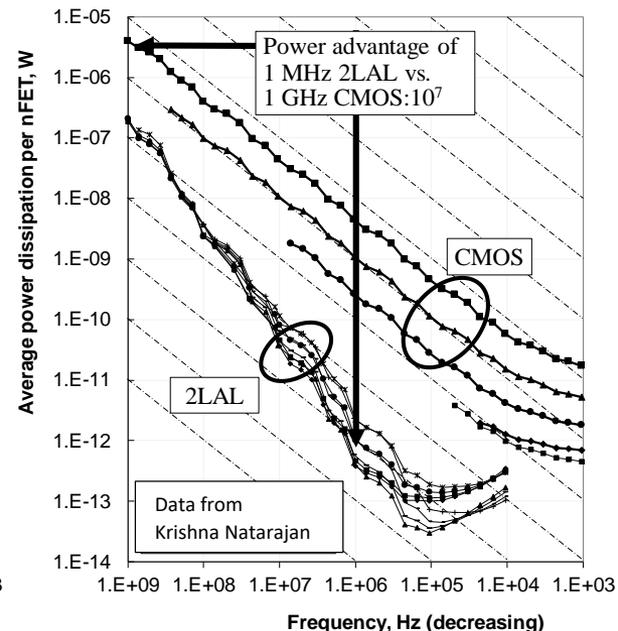
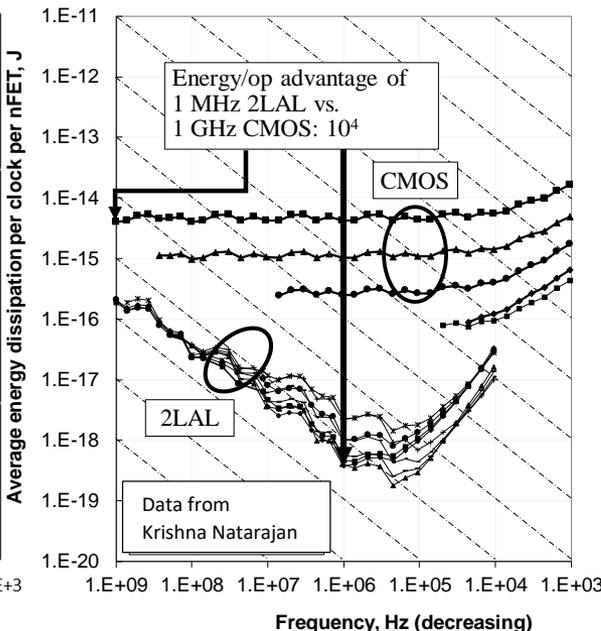
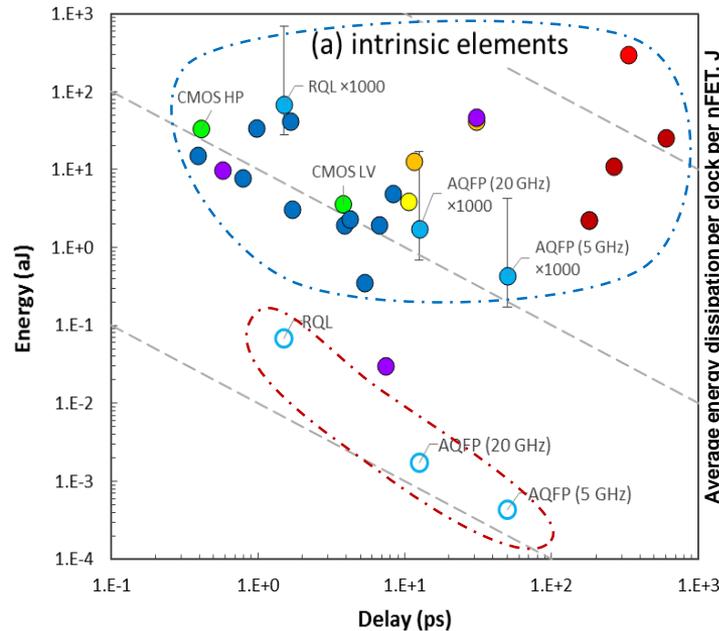


Cryo CMOS vs. CATC I

- All transistor circuits have $\frac{1}{2}CV^2$ signal energy
- Adiabatic 2LAL dissipates less in the chip
- How is that possible given conservation of energy?

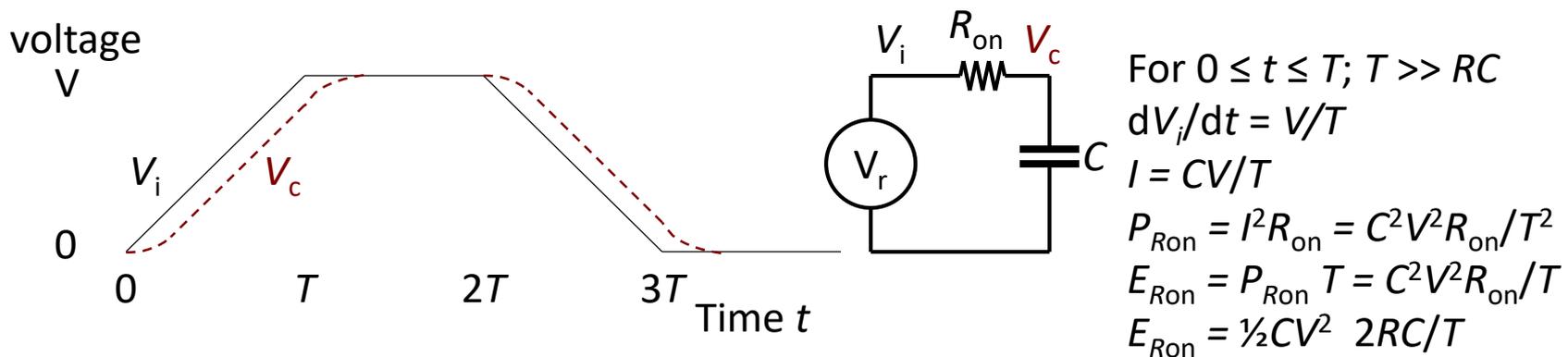
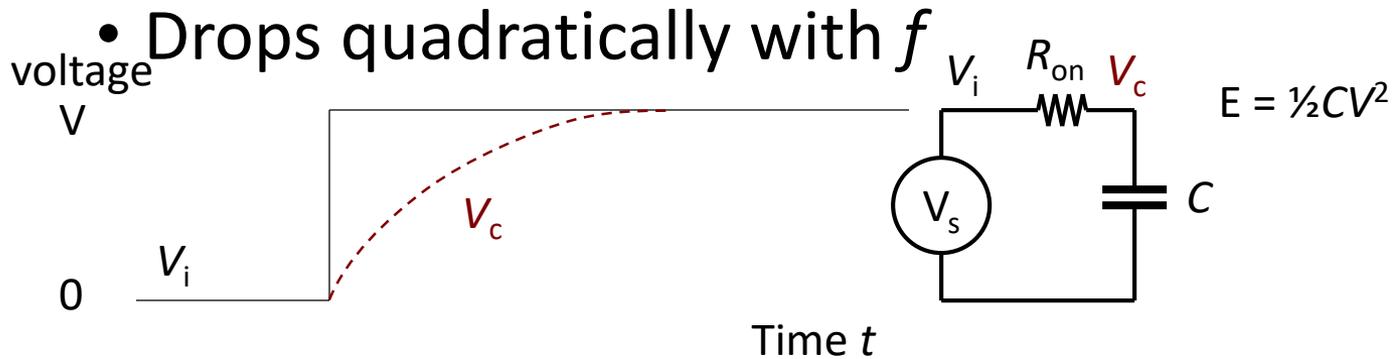
Energy/op vs. freq., TSMC 0.18, CMOS vs. 2LAL

Power/device vs. freq., TSMC 0.18, CMOS vs. 2LAL

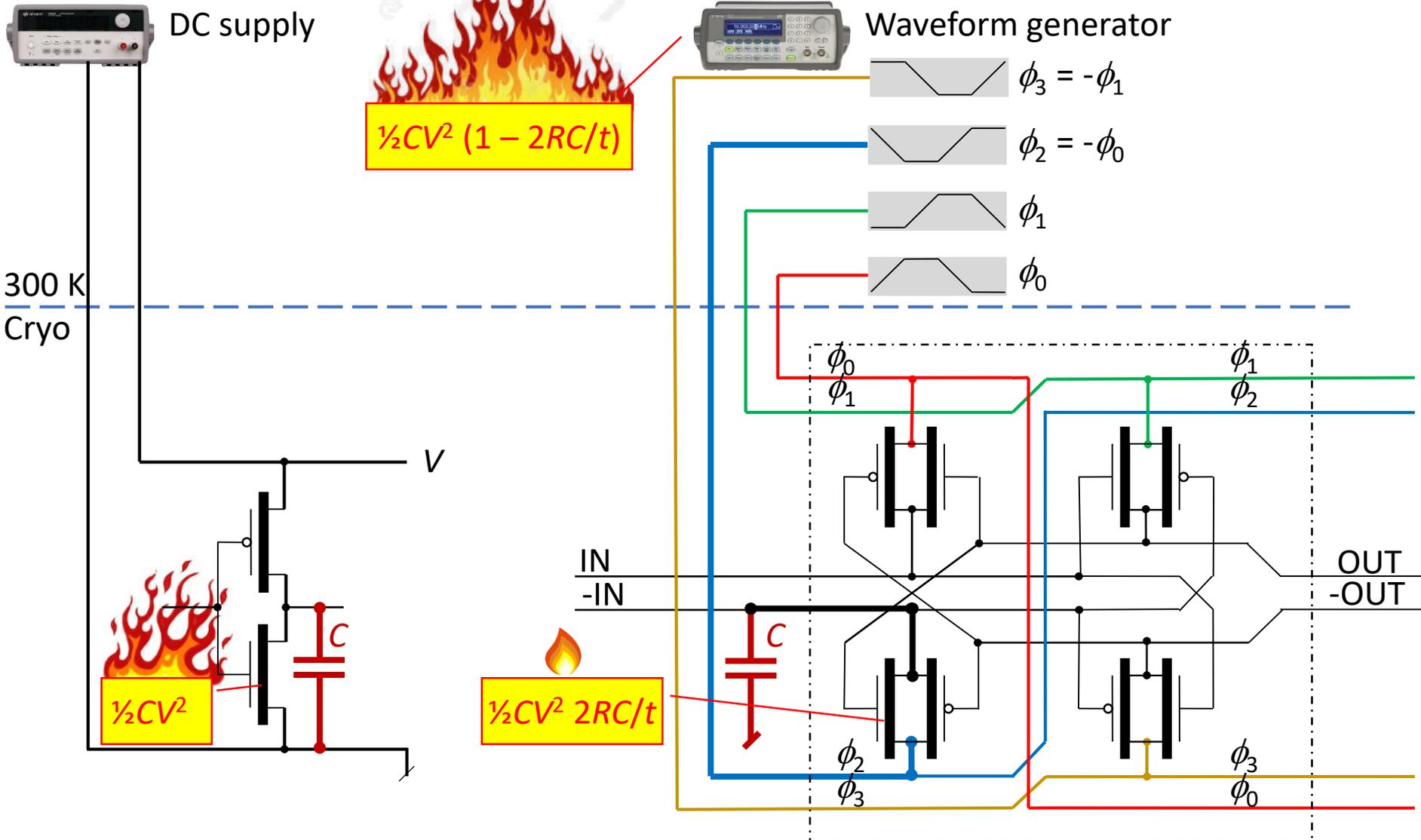


Backup: RC Charging

- CMOS: Energy per transition $E = \frac{1}{2}CV^2$ always
- Adiabatic charging: $\{ \frac{1}{2}CV^2 \} \{ 2RC/T \}$ for large T
- Drops quadratically with f



Cryo CMOS vs. CATC II



Backup: Transistor changes

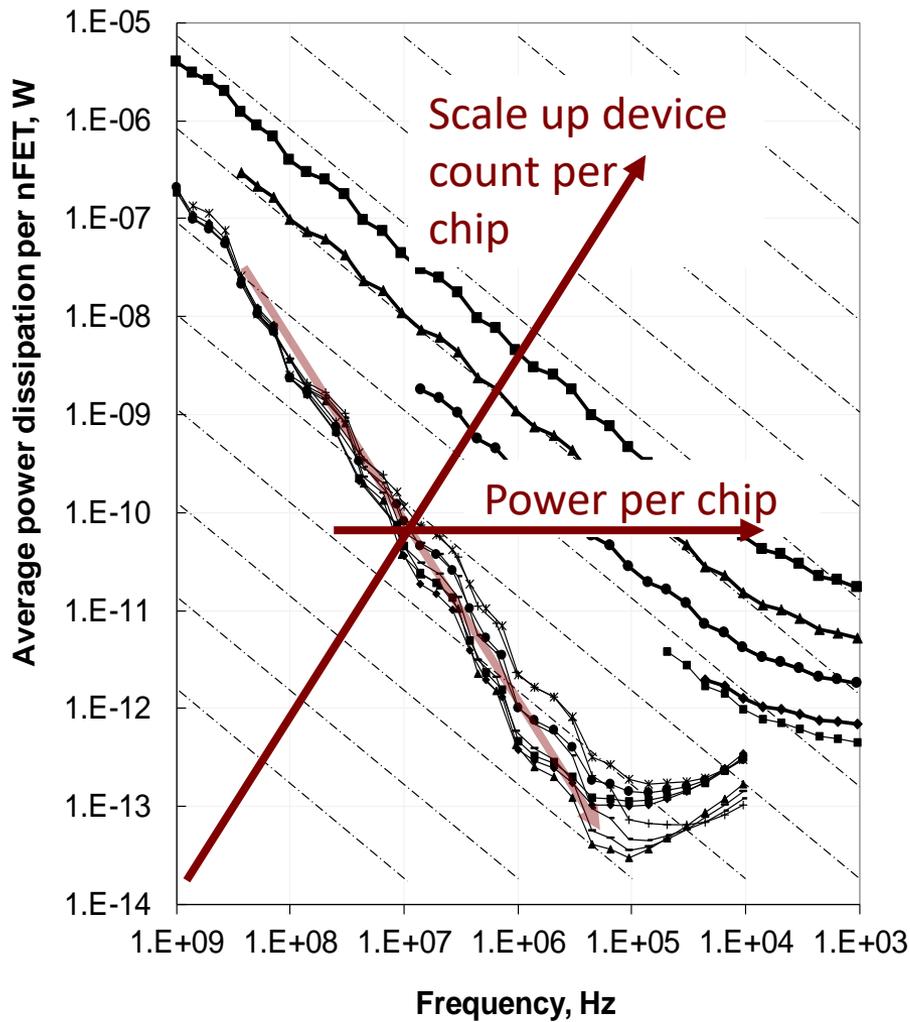
- Transistors used to experience carrier freeze out and 'kinks,' but these effects are no longer a problem due to the natural evolution of transistors
- Some DRAMs and some FPGAs work at 4 K now
 - See for example, FPGA Design Techniques for Stable Cryogenic Operation, arXiv:1709.04190
- This validates that cryo CMOS can work at 4 K
 - Except for imposing a refrigeration load
- New transistor lines for IoT are on the right path
 - Intel 22FFL, GF 22FDX, TSMC 22ULP, or ST 28 FDSOI

Backup: Basic physics of cooling

- Electric energy is happy to flow through a wire that crosses a temperature gradient in either direction
- Heat flows to a lower temperature unassisted, but needs energy to move to a higher temperature
- Reversible and adiabatic computing tried to recycle energy within a single-temperature system, but the necessary energy-recycling power supply has not been found after decades of looking
- Cryogenic adiabatic transistor circuits move waste across the temperature gradient as energy before turning it into heat, not after

Adiabatic scaling

Power/device vs. freq., TSMC 0.18, CMOS vs. 2LAL



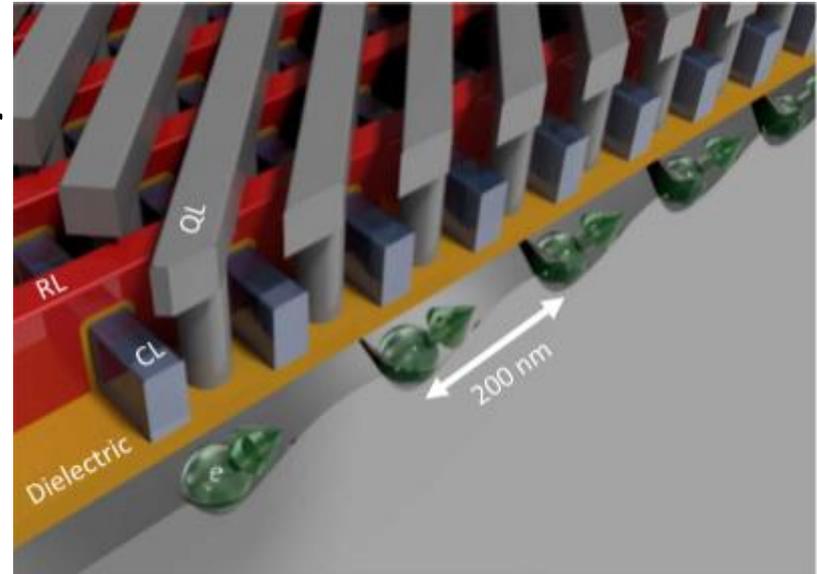
- Scale up clock period – i. e. slow the clock
- Per-gate dissipation drops quadratically
- But add quadratically more devices at same total power
- No free lunch
 - Supply current rises
 - Transistor leakage
 - Run out of chip space

Question of the hour

- Can cryogenic adiabatic transistor circuits become the memory counterpart for JJ/SFQ?
- If we follow adiabatic scaling, will ...
 - device count rise enough to comprise a “memory”
 - before speed makes it unusably slow?

Hybrid Semi- Superconductor

- Conventional wisdom is that an all-semiconductor quantum computer would be most elegant
- Example on right is 100% semiconductor, except for the superconductor wires (CL and QL)
- From Li, Ruoyu, et al. "A crossbar network for silicon quantum dot qubits." *Science advances* 4.7 (2018): eaar3960. (5 of 14 authors from Intel)

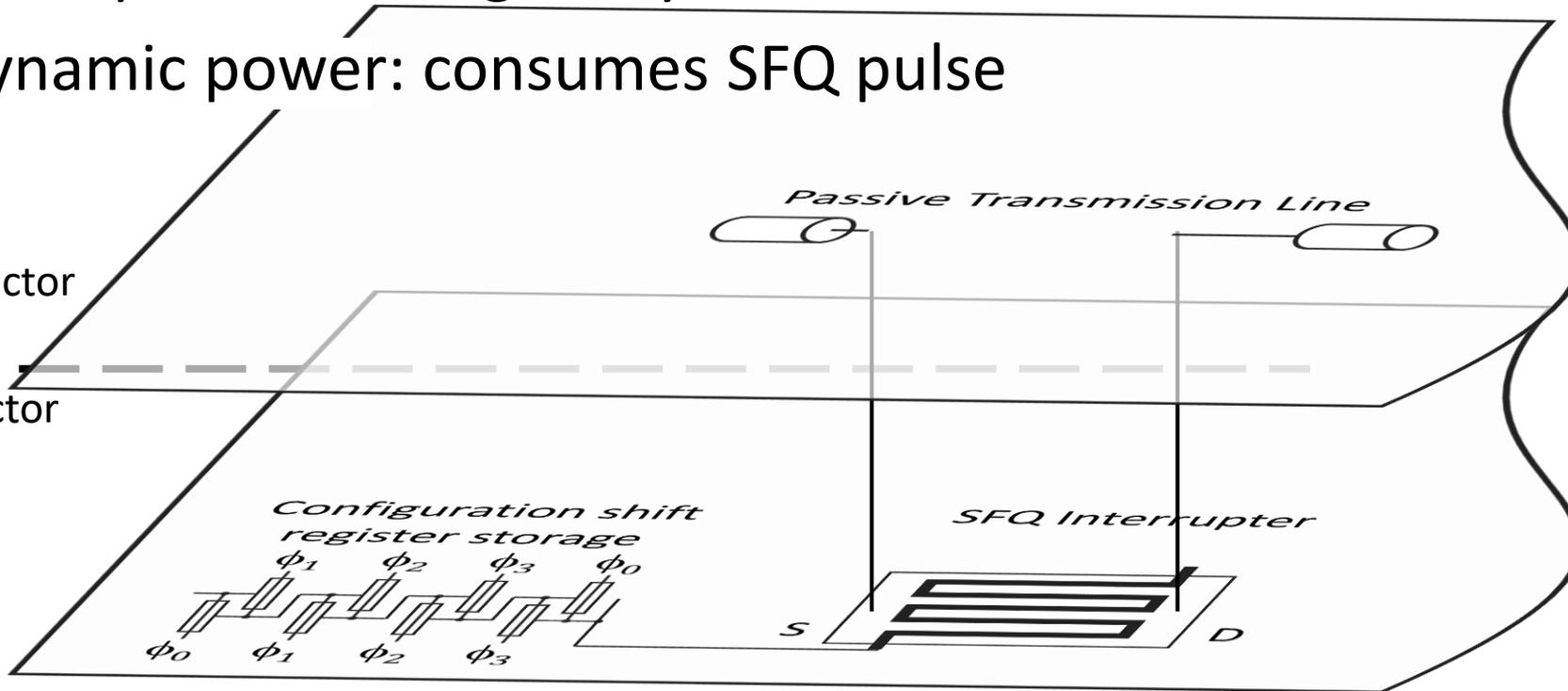


Cross-layer Interface (basic)

- Energy-recovering logic feeds gate of big transistor
- Transistor passes or blocks SFQ pulse (10s of Ohms)
- Static power: leakage only
- Dynamic power: consumes SFQ pulse

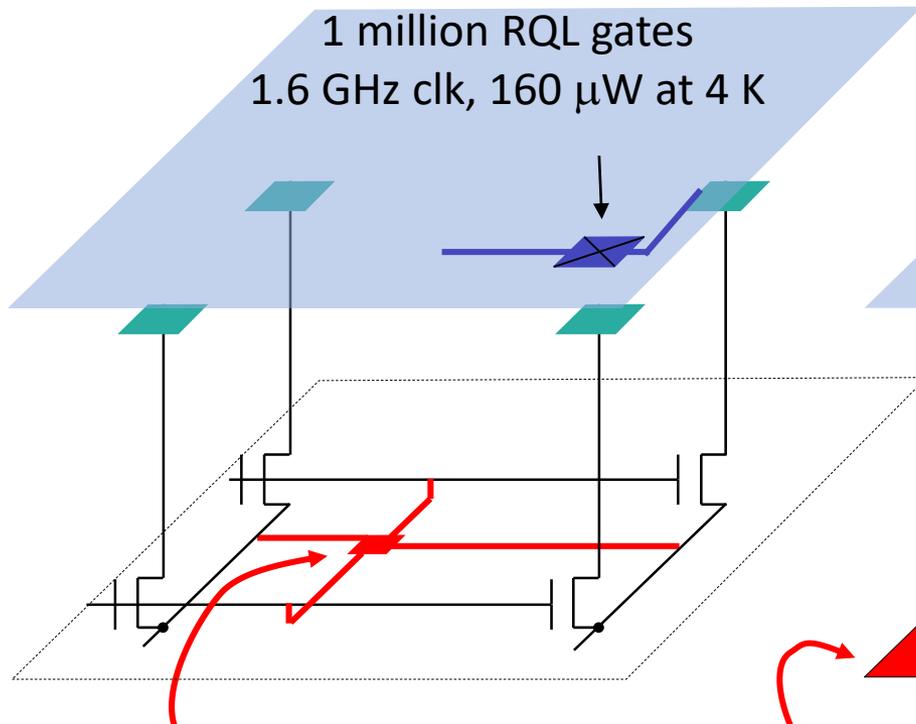
Superconductor
layer

Semiconductor
layer

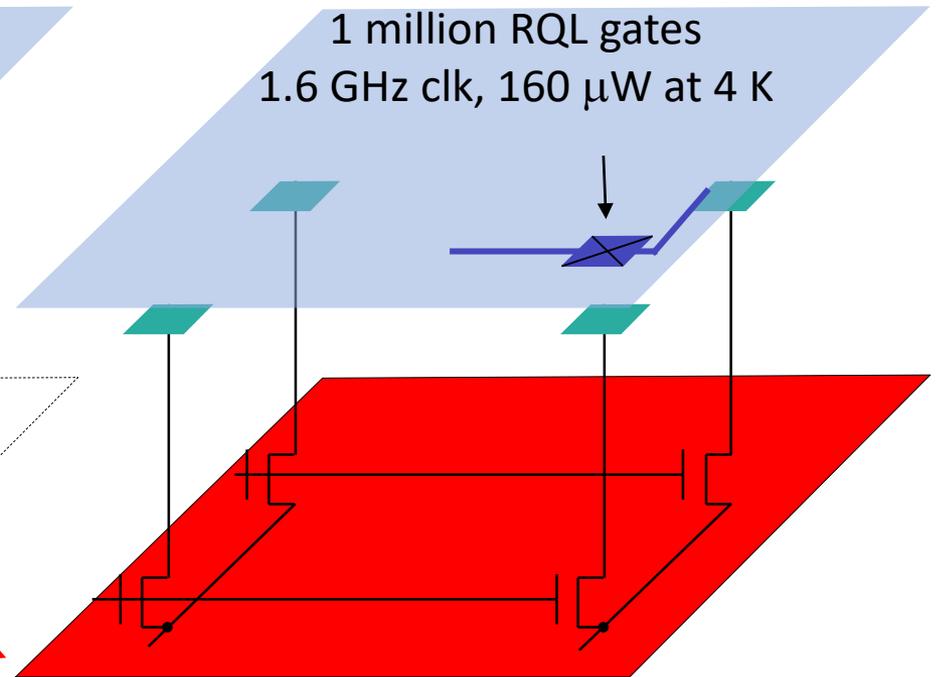


Scaling summary

Baseline



Scaling step 3



1,000 cryo CMOS gates (to scale)
4 GHz clk, 160 μ W at 4 K

100 million 2LAL gates (to scale)
4 MHz clk, 160 μ W + 167 μ W (leakage) at 4 K

Backup: JJ-2LAL scaling steps I

- Each step: 100× gates; 1/10 clock rate; same chip power; static leakage rises with device count
- First step CMOS → 2LAL 10× device penalty

Baseline	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
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	$N_{\text{CMOS}} = 1 \text{ K}$	$f_{\text{CMOS}} = 4 \text{ GHz}$	$P_{\text{CMOS}} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
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Scaling Step 1	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
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	$N_{\text{2LAL}}^{(1)} = 10 \text{ K}$	$f_{\text{2LAL}}^{(1)} = 400 \text{ MHz}$	$P_{\text{2LAL}}^{(1)} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}}^{(1)} = 16.7 \text{ nW}$
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Scaling Step 2	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
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	$N_{\text{2LAL}}^{(2)} = 1 \text{ M}$	$f_{\text{2LAL}}^{(2)} = 40 \text{ MHz}$	$P_{\text{2LAL}}^{(2)} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}}^{(2)} = 1.67 \text{ } \mu\text{W}$
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Scaling Step 3	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
----------------	--------------------------------	------------------------------------	---	----------------------------------

	$N_{\text{2LAL}}^{(3)} = 100 \text{ M}$	$f_{\text{2LAL}}^{(3)} = 4 \text{ MHz}$	$P_{\text{2LAL}}^{(3)} = 160 \text{ } \mu\text{W}$	$P_{\text{Static}}^{(3)} = 167 \text{ } \mu\text{W}$
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Backup: JJ-2LAL scaling steps II

- Each step: 100× gates; 1/10 clock rate; same chip power; static leakage rises with device count
- First step CMOS → 2LAL 10× device penalty

Baseline	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
	$N_{\text{CMOS}} = 1 \text{ K}$	$f_{\text{CMOS}} = 4 \text{ GHz}$	$P_{\text{CMOS}} = 160 \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
	Device count rises 10^5	Speed drops 1,000×	Chip is now full; power rises 3×	
Scaling Step 3	$N_{\text{RQL}} = 1 \text{ M}$	$f_{\text{RQL}} = 1.6 \text{ GHz}$	$P_{\text{RQL}} = 160 \mu\text{W}$	$P_{\text{Static}} = \text{n/a}$
	$N_{\text{2LAL}}^{(3)} = 100 \text{ M}$	$f_{\text{2LAL}}^{(3)} = 4 \text{ MHz}$	$P_{\text{2LAL}}^{(3)} = 160 \mu\text{W}$	$P_{\text{Static}}^{(3)} = 167 \mu\text{W}$

JJ μ wave Components

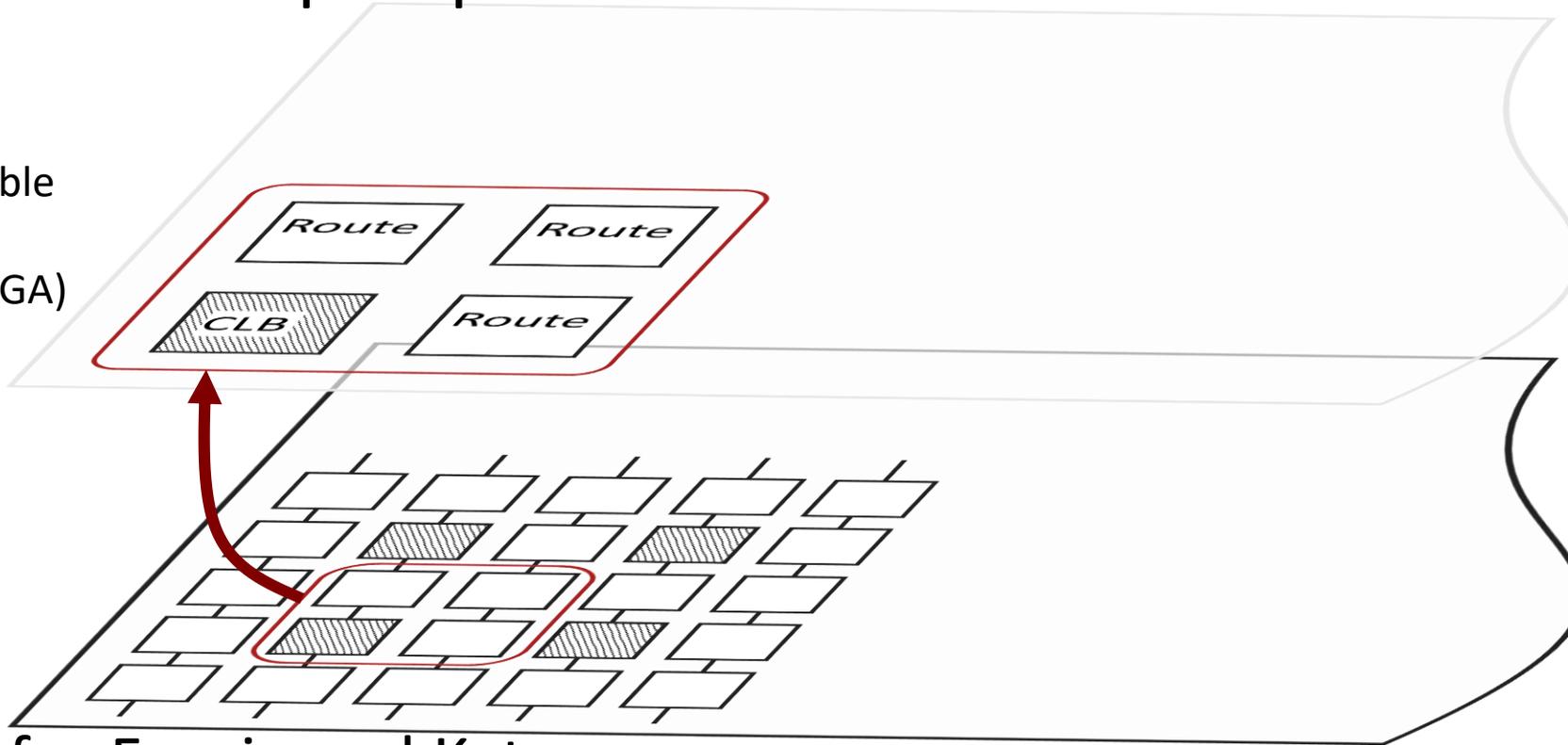
μ wave SPST
switch



- There is a need to control microwaves at cryo
 - Northrop-Grumman, Google (Naaman)
 - Transmon quantum computers, etc.
- However, all current options require control signals from room temperature, limiting scalability

JJ FPGAs proposed

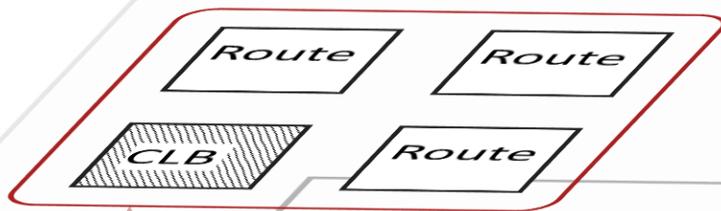
Reconfigurable
Josephson
junction (FPGA)



- Refs.: Fourie and Katam
- However, the configuration logic is via JJs, so the result is not very dense

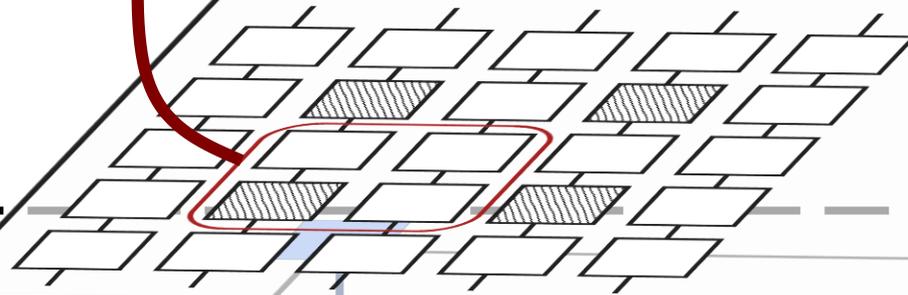
Hybrid 2LAL-JJ controller

Reconfigurable
Josephson
junction (FPGA)

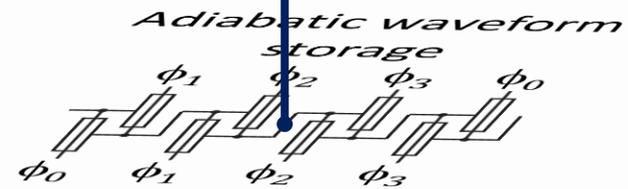
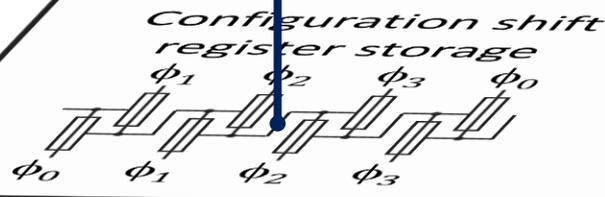


Controlled
layer

Configuration
layer

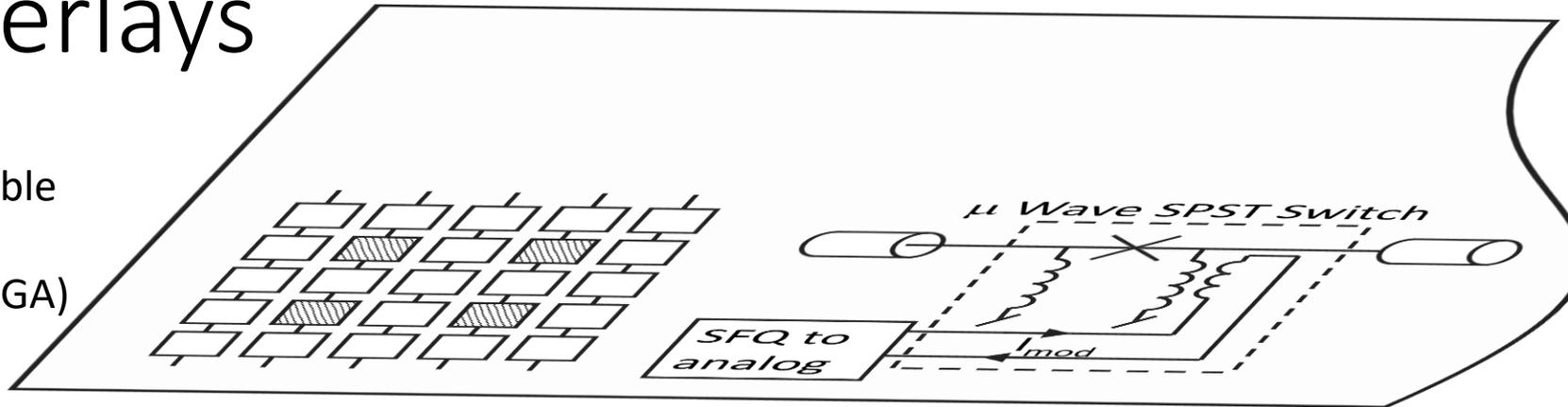


Adiabatic shift
register
memory

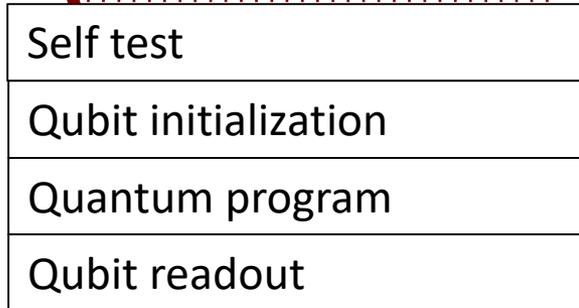


Quantum program with FPGA overlays

Reconfigurable Josephson junction (FPGA)



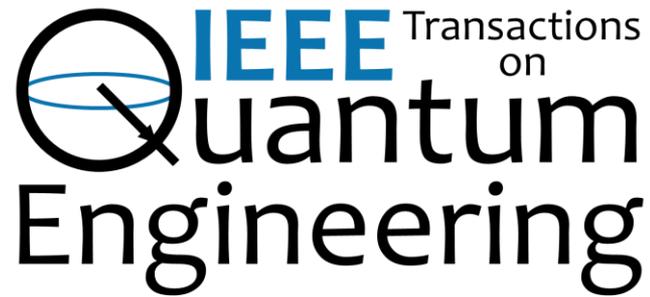
Program via FPGA overlay



- Reconfiguration time estimate 250 ns
- Qubit decoherence time 10s of μ s
- Qubit state can persist across a reconfiguration

Conclusions

- Paper <http://www.zettaflops.org/CATC>
- Pre quantum supremacy brings attention to scalable control systems for quantum computes
- Cryogenic adiabatic transistor circuits are helpful due to a principle related to temperature
 - “dissipate the heat at 300 K”
- System designers expect a suite of technologies
 - Smartphones need CMOS + DRAM + Flash
 - Cryo systems need JJs + Cryo adiabatic transistor circuits
- Further work:
 - Test hybrid of JJ + 22FFL, 22FDX, 22ULP, or ST 28 FDSOI
 - Test architectures applicable to quantum computer control
 - Rebalance transistors

The logo for IEEE Transactions on Quantum Engineering. It features a stylized 'Q' on the left, composed of a circle with a horizontal line and a diagonal line. To the right of the 'Q', the text 'IEEE' is in blue, 'Transactions' is in black above 'on', and 'Quantum Engineering' is in black below 'on'.

Status: Proposed for approval November 2019, first issue January 2020

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Scope: TQE covers quantum engineering within IEEE’s scope of electrical and electronic engineering.



Backup

Backup: Transistor properties

- Based on Spice simulations, 4 K quantum computer controllers need to scale 50-72 qubits to the next step should work with Intel 22FFL, GF 22FDX, TSMC 22ULP, ST 28 FDSOI “out of box”
- Custom transistors would help, may not be that different
 - Need ultra-low leakage, i. e. high I_{on}/I_{off} ratio
 - Quantum computer performance comes from the qubits, so the traditional CMOS metrics don't hold
 - Natural steepening of subthreshold slope give maneuvering room; need thicker oxide and threshold adjustment at some point

Backup: Architectural issues

(Cryogenic Adiabatic Transistor Circuit = CATC)

- The CATC advantage is narrow
 - CATCs are slow; need to be a hybrid with something fast to be useful. Fortunately, a CATC-JJ hybrid is natural
 - Memory needs to be dense. Fortunately, CATCs are nearly as dense as transistors, far denser than JJs
 - CATCs are not fast enough to be the addressing logic for RAM, but CATCs work for memory-like structures like shift registers
- FPGAs and buffers
 - Quantum computer controllers are halfway between signal processors and general purpose computers

Backup Cold, scalable controller

- Hybrid FPGA
 - Configured logic: JJs, configuration logic: transistors
 - Problem: JJs are huge
 - Solution: FPGA “timeshares” JJs by on-the-fly reconfiguration
- All-cold SFQ microwave components
 - There is a suite of switches, modulators, etc. available, but they require waveforms piped in from 300 K
 - While we don't know how to make a random access cryo memory, waveforms are accessed as a stream, making the shift register in previous slides sufficient