Differential Power Analysis of a Fully Adiabatic Circuit

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December 19, 2020

Document ZF007

Overview I

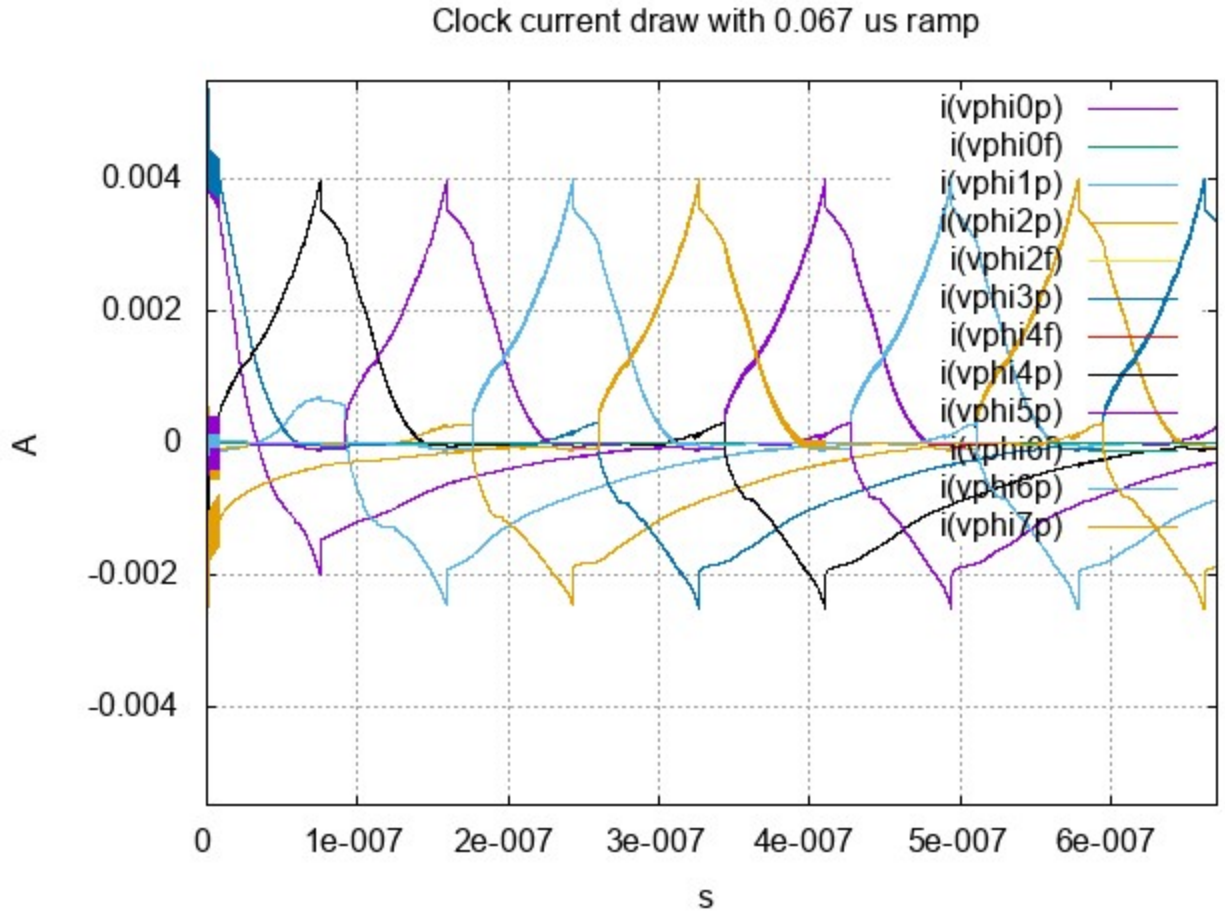
- Adiabatic circuits that have been studied for performance under differential power analysis produce current spikes when signals drop below v_t
- As clock rate lengthens
  - adiabatic dissipation drops
  - spikes due to v_t do not change
- Differential power analysis ends up measuring the high-speed switching characteristics of transistors
- A fully adiabatic circuit could be expected to have
  - lower functional dissipation at lower speeds
  - no v_t spike
  - current increasingly independent of some transistor characteristics at slow speeds
- Let's see

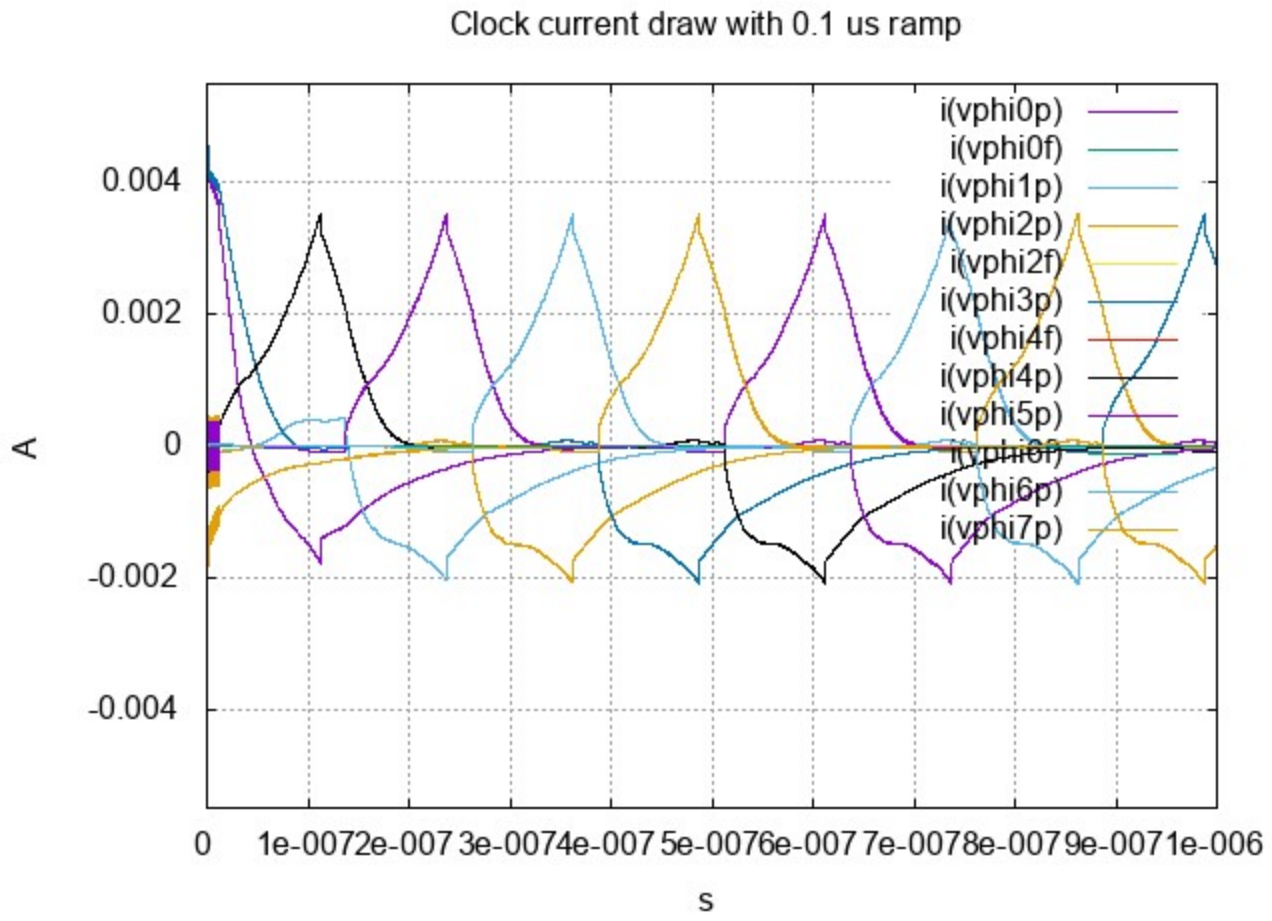
Overview II

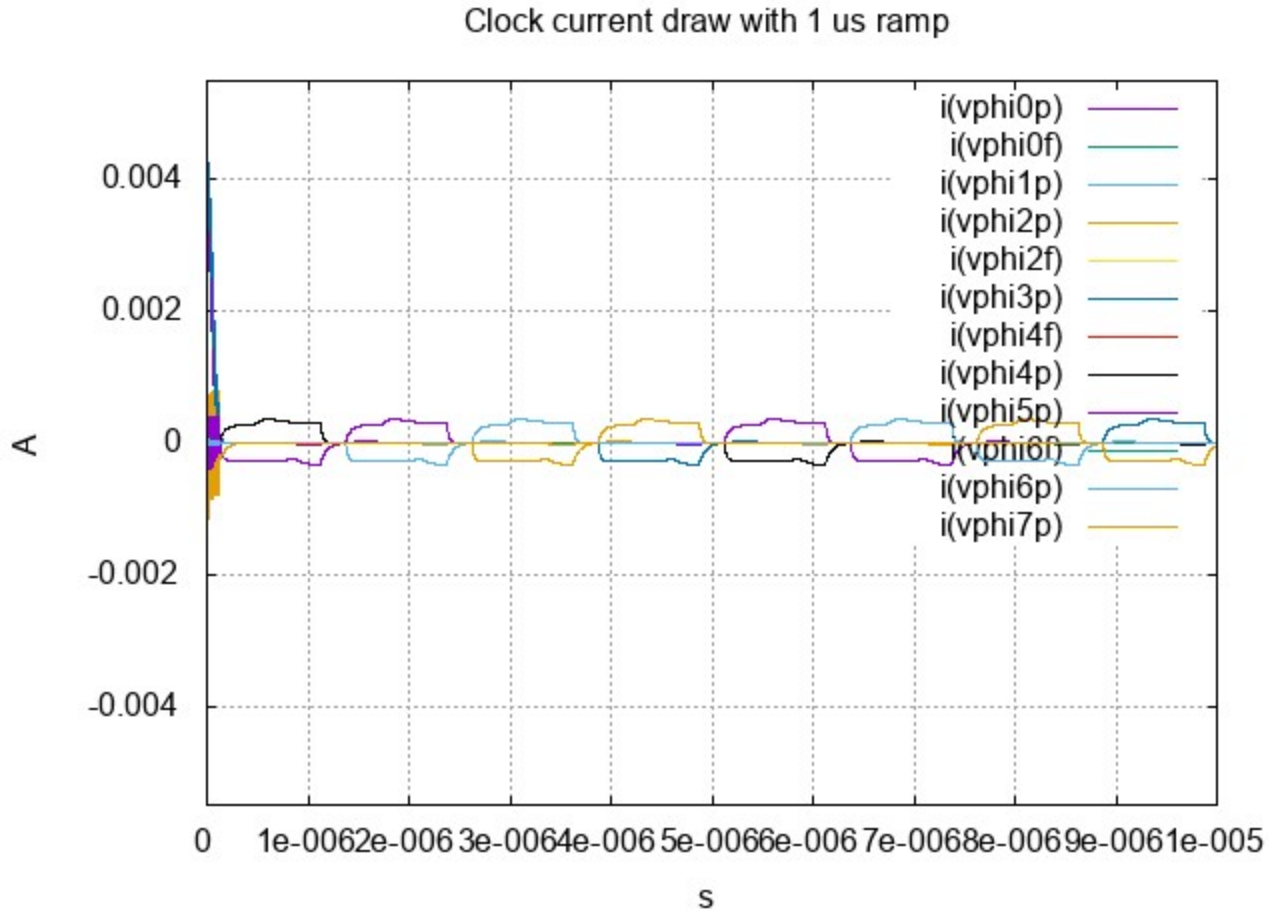
- Mike Frank's S2LAL is fully adiabatic
  - However, 1s are represented by pulses and 0s by DC levels
  - So 1s dissipate more power than 0s (in a dual rail system)
  - Mike pointed out to me that switching to quad rail addresses the issue
- Erik DeBenedictis developed a variant where 0s and 1s are represented by pulses on different rails
  - a dual-rail system could have current draw independent of data
  - this circuit is described in ZF005 on https://zettaflops.org/CATC
  - the variant is tentatively named Q2LAL for "quiet 2LAL"

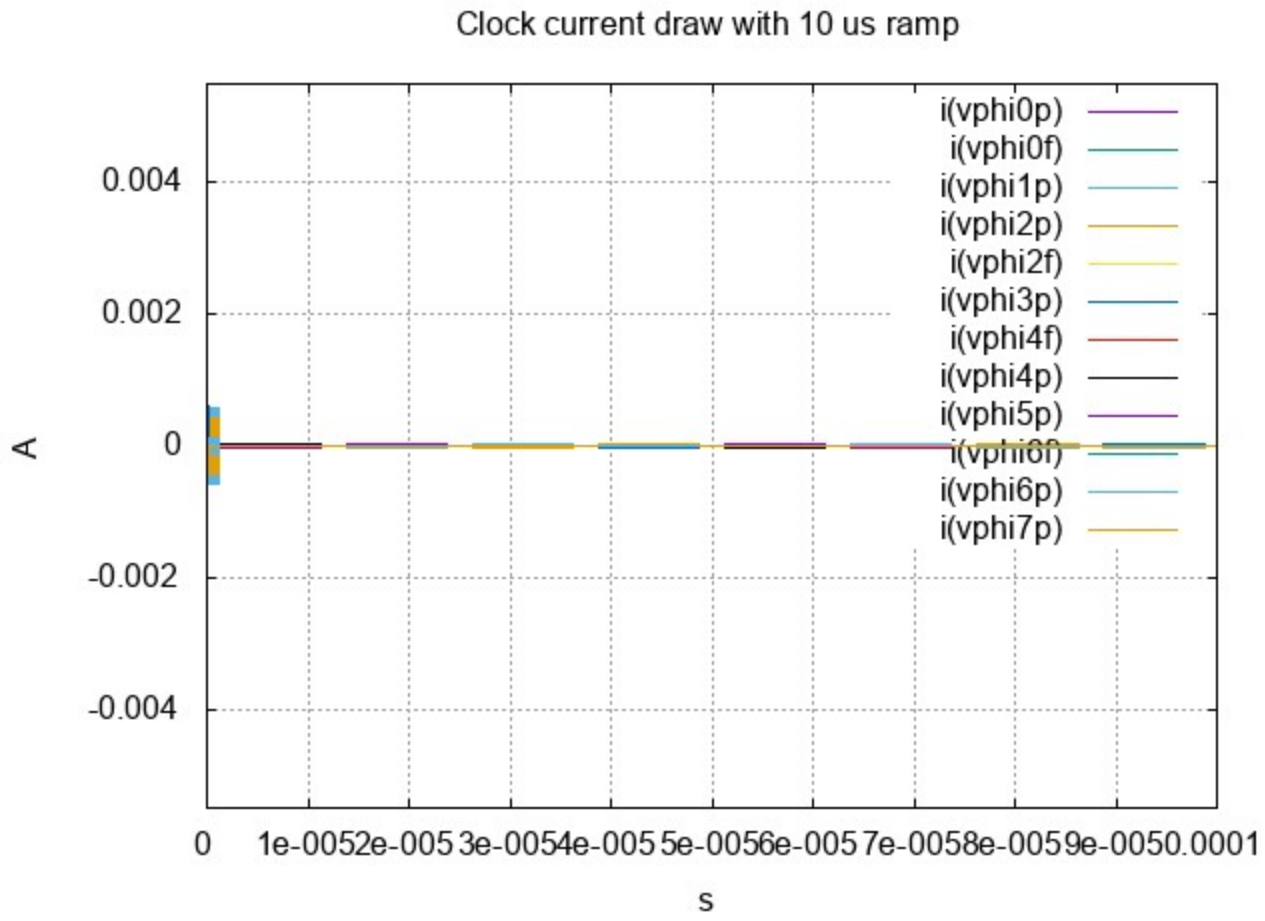
Four Spice Waveforms

- Subsequent four slides have waveforms of clock current at
  - 67 ns ramp
  - 100 ns ramp
  - 1 μs ramp
  - 10 μs ramp
- The slides look the same, so page through in PowerPoint like an animation
  - each graph shows one full eight-phase clock
  - the horizontal axis and the clock rate have been scaled by the same amount
- This is simulation using the ngspice built-in transistor model; only circuit properties should be considered
- Circuit described in ZF005 on https://zettaflops.org/CATC


Clock current draw with 0.067 us ramp
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)
0.004
0.002
0
-0.002
-0.004
A
0
1e-007
2e-007
3e-007
4e-007
5e-007
6e-007
s

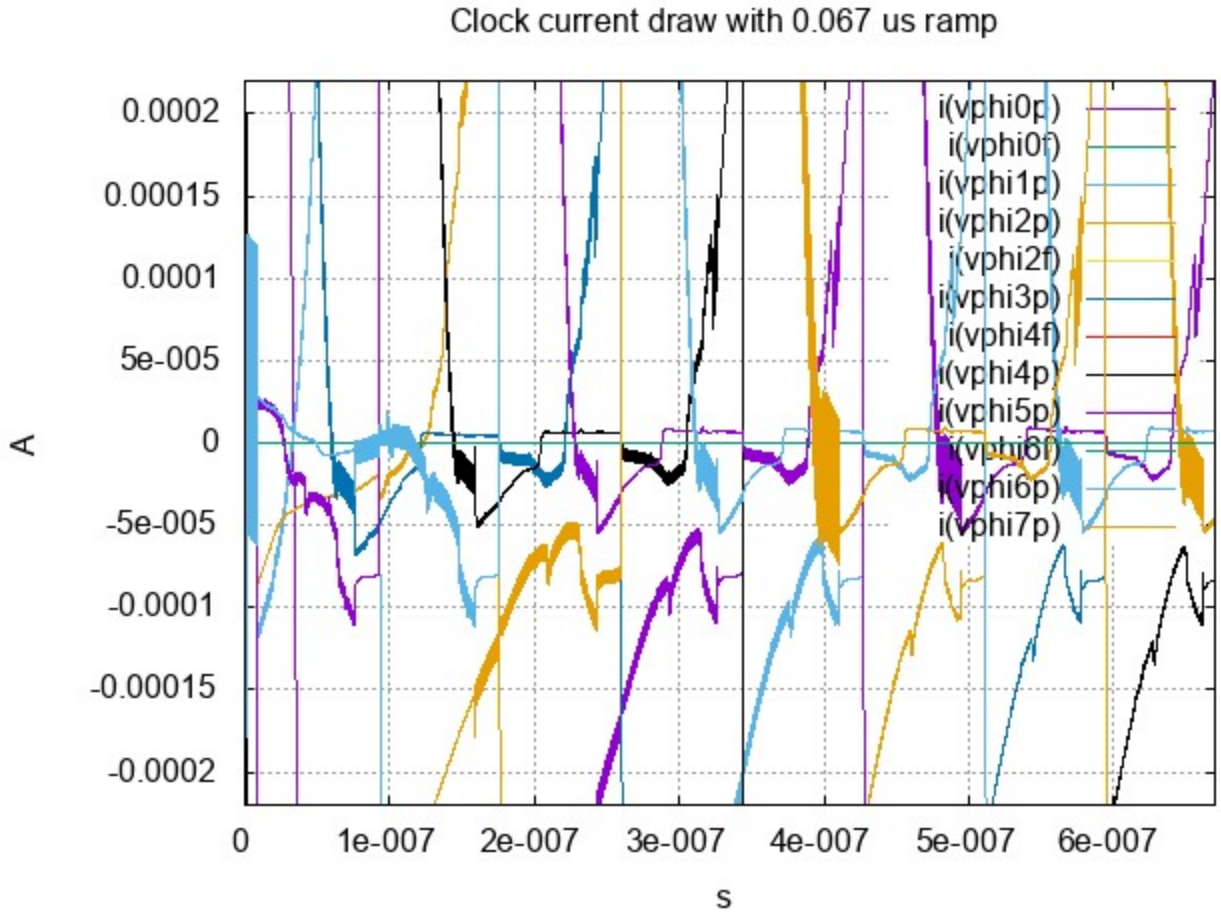

Clock current draw with 0.1 us ramp
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6p)
i(vphi7p)
0.004
0.002
0
-0.002
-0.004
A
0
1e-007
2e-007
3e-007
4e-007
5e-007
6e-007
7e-007
8e-007
9e-007
1e-006
s

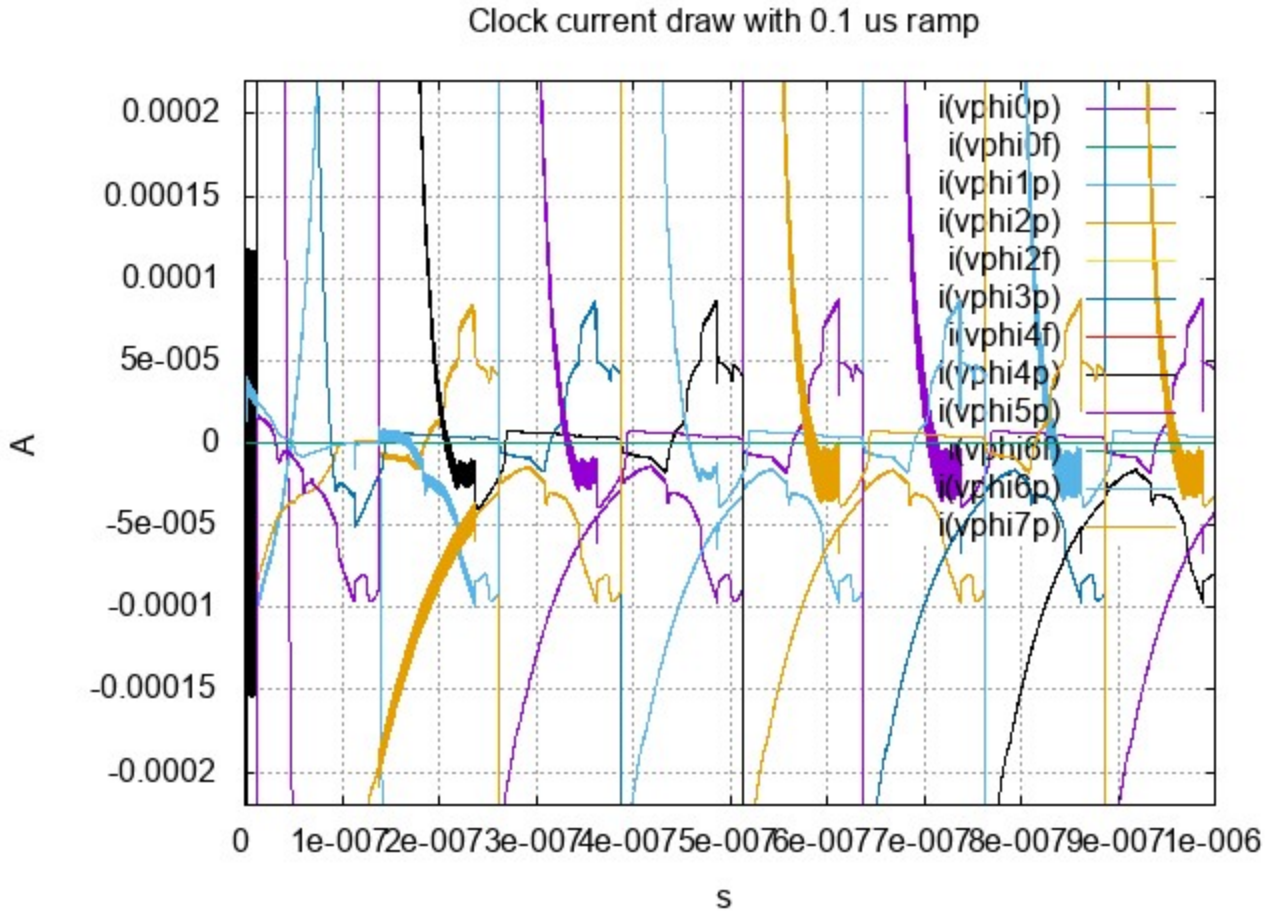

Clock current draw with 1 us ramp
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)
0.004
0.002
0
-0.002
-0.004
A
0
1e-006
2e-006
3e-006
4e-006
5e-006
6e-006
7e-006
8e-006
9e-006
1e-005
s

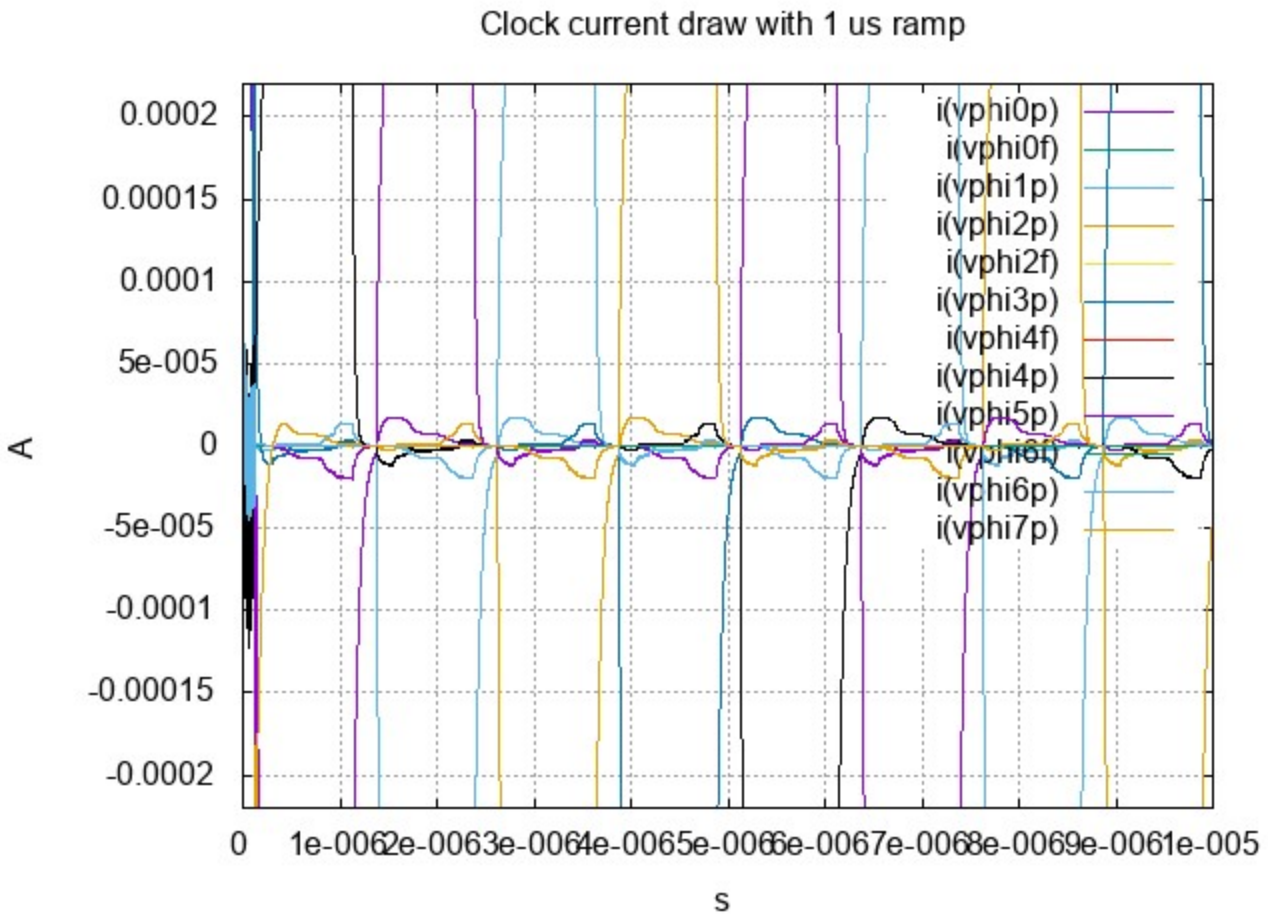

Clock current draw with 10 us ramp
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)
0.004
0.002
0
-0.002
-0.004
A
0
1e-005
2e-005
3e-005
4e-005
5e-005
6e-005
7e-005
8e-005
9e-005
0.0001
s

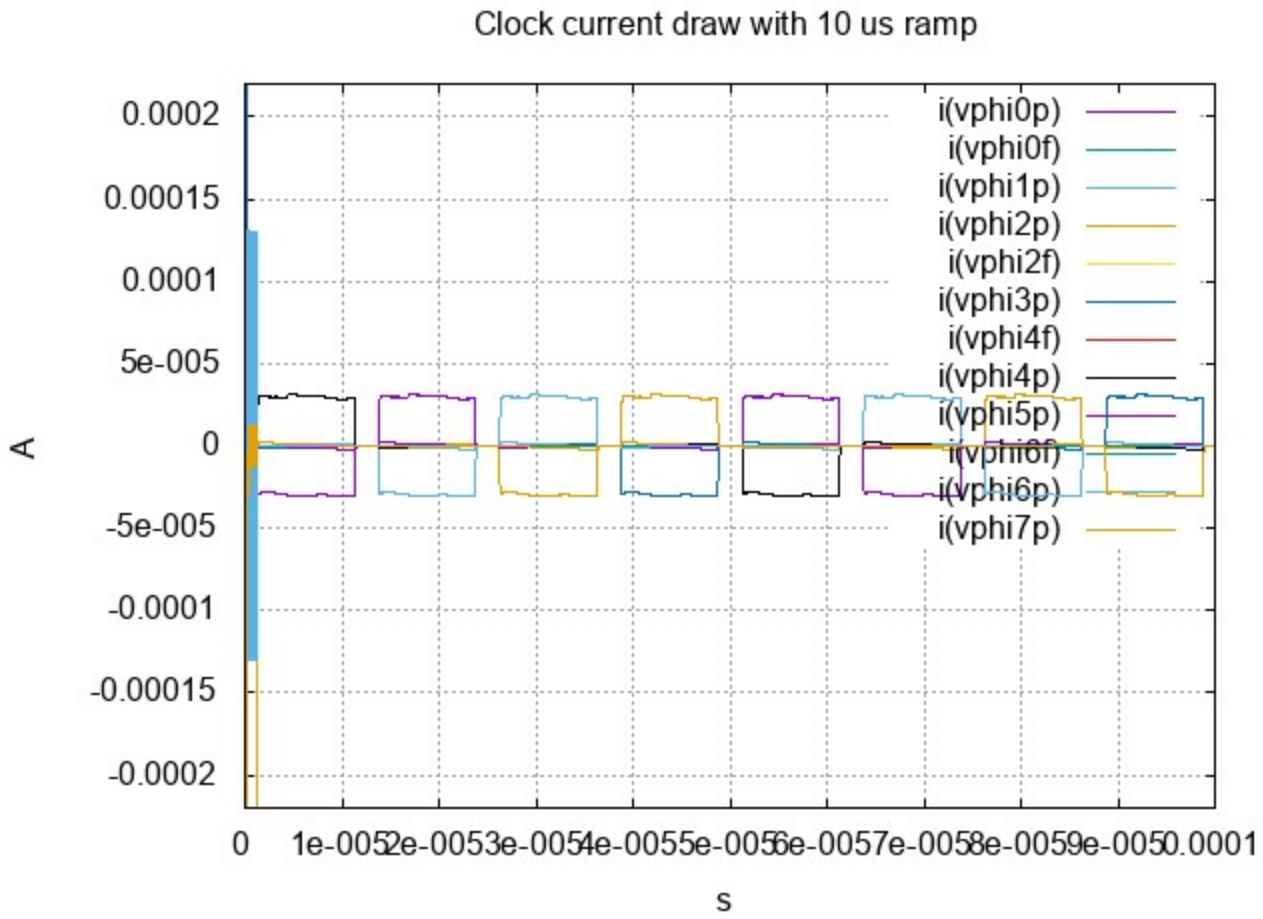
Four waveforms

- Let’s repeat the same simulation with 10× larger vertical scale
- Note the final waveform is very clean


Clock current draw with 0.067 us ramp
0.0002
0.00015
0.0001
5e-005
0
-5e-005
-0.0001
-0.00015
-0.0002
A
0
1e-007
2e-007
3e-007
4e-007
5e-007
6e-007
s
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)

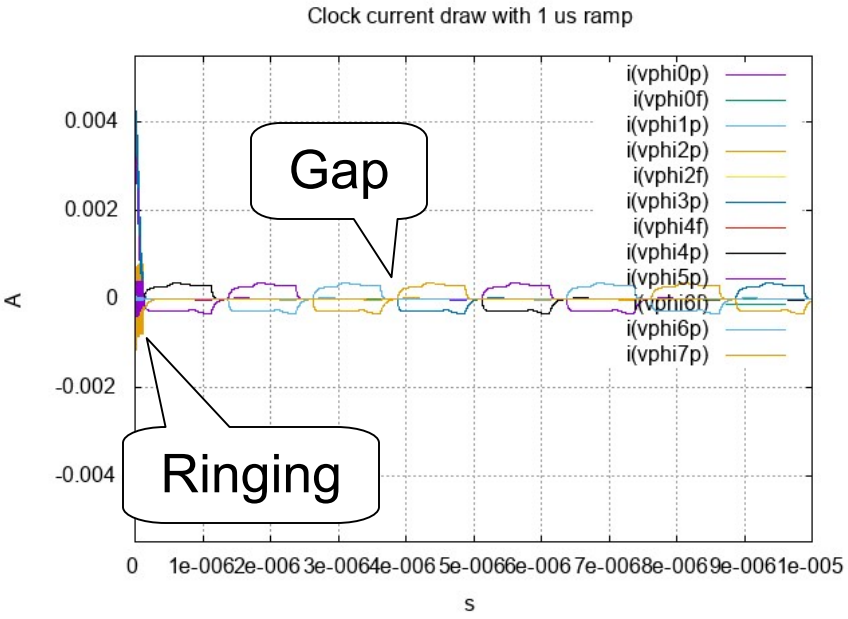

Clock current draw with 0.1 us ramp
A
s
0.0002
0.00015
0.0001
5e-005
0
-5e-005
-0.0001
-0.00015
-0.0002
0
1e-007
2e-007
3e-007
4e-007
5e-007
6e-007
7e-007
8e-007
9e-007
1e-006
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)

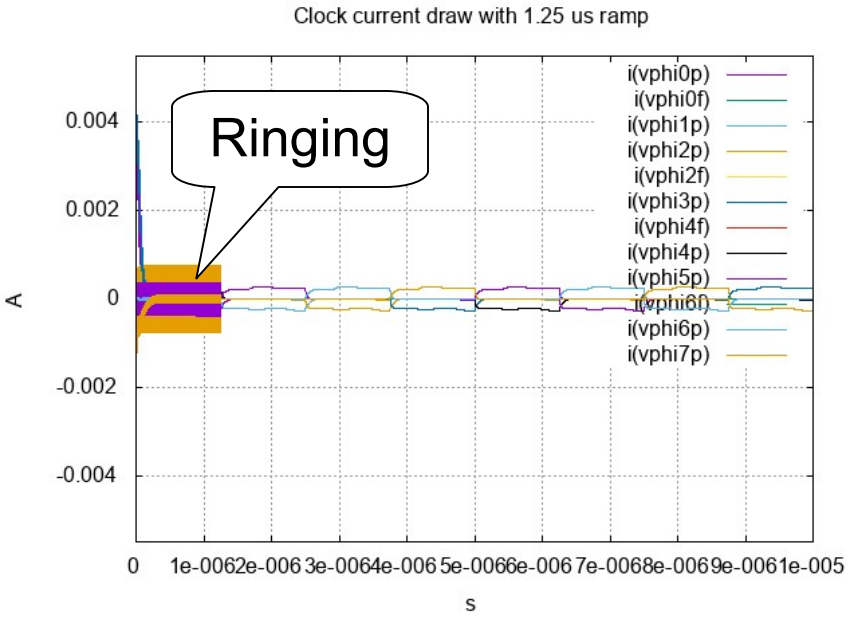

Clock current draw with 1 us ramp
0.0002
0.00015
0.0001
5e-005
0
-5e-005
-0.0001
-0.00015
-0.0002
A
0
1e-006
2e-006
3e-006
4e-006
5e-006
6e-006
7e-006
8e-006
9e-006
1e-005
s
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)


Clock current draw with 10 us ramp
0.0002
0.00015
0.0001
5e-005
0
-5e-005
-0.0001
-0.00015
-0.0002
A
0
1e-005
2e-005
3e-005
4e-005
5e-005
6e-005
7e-005
8e-005
9e-005
0.0001
s
i(vphi0p)
i(vphi0f)
i(vphi1p)
i(vphi2p)
i(vphi2f)
i(vphi3p)
i(vphi4f)
i(vphi4p)
i(vphi5p)
i(vphi6f)
i(vphi6p)
i(vphi7p)

Clock Gap and Ringing

- The simulation has been programmed with a programmable gap between clocks, set to 20% in other slides
- The gap has been removed on the right graph below
- The ringing on the left seems to be instability in ngspice





Backup: ngspice code

- The ngspice source to the right in 1 point font was used to generate the content of this deck
- To reproduce the results, scrape the source from a pdf rendering
- To reproduce results, see also document ZF005 on https://zettaflops.org/CATC