Inversion for S2LAL

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Abstract

This brief technical note is in response to the recently introduced S2LAL[1] logic family, which is a static version of the 2LAL family.[2] I created an inverter for 2LAL in a previous report,[4] and create an inverter for S2LAL here using similar principles. S2LAL as described in ref. 1 requires quad-rail logic because there is no other source of inversion. With the inversion in this note, quad-rail logic can still be used but is not necessary. The use of inversion will result in much small circuits in important cases.

S2LAL Inverter

The 2LAL and S2LAL inverters use the same principle. For 2LAL, I created a 2-level clock cascade, which had the disadvantage of extending the cycle from 4 to 6 ramps. However, S2LAL already contains the equivalent 2-level cascade in the sense that ϕ_2 fits entirely within the flat top of S_1. In fig. 1, I repeat the method of using a "0" data signal S_1 to gate clock ϕ_2, which has the same initial shape as a "1" signal, thus inverting S_1.

During forward clocking, each stage is expected to drive the S_2 signal when ϕ_1 is high, making the transition from 0 to 1 (if there is to be a transition) at the same time as the ϕ_2 clock. The stage is expected to be tri-stated when ϕ_1 is low. The circuit complies.

The intermediate signal X is created by using S_1 to multiplex between ϕ_2 and ground. The timing diagram shows that the ϕ_2 clock transition occurs when the S_1 signal is stable, so the X signal is always a low-impedance voltage source and can deliver or recover energy. The pass gate to a fixed voltage could be replaced by a single transistor, as in ref. 1.

The circuit in fig. 1 is shorthand for a pair of circuits with complementary voltages. All indices may be shifted, mod 8, allowing inversion to occur in any phase.

The circuit is not exactly an inverter; it takes a stream of bits and creates a second stream with the logical complement of the bits. As in ref. 4, this type of circuit runs backwards naturally and can be mirrored.

References

[1] Frank, Michael P., et al. "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS." *arXiv preprint arXiv:2009.00448* (2020).

[2] V. Anantharam, M. He, K. Natarajan, H. Xie, and M. P. Frank. "Driving fully-adiabatic logic circuits using custom high-Q MEMS resonators," in *Proc. Int. Conf. Embedded Systems and Applications and Proc. Int. Conf VLSI (ESA/VLSI)*. Las Vegas, NV, pp. 5-11.

[3] *Enhancements to Adiabatic Logic for Quantum Computer Control Electronics*. Zettaflops LLC technical report ZF002, http://www.zettaflops.org/CATC/.

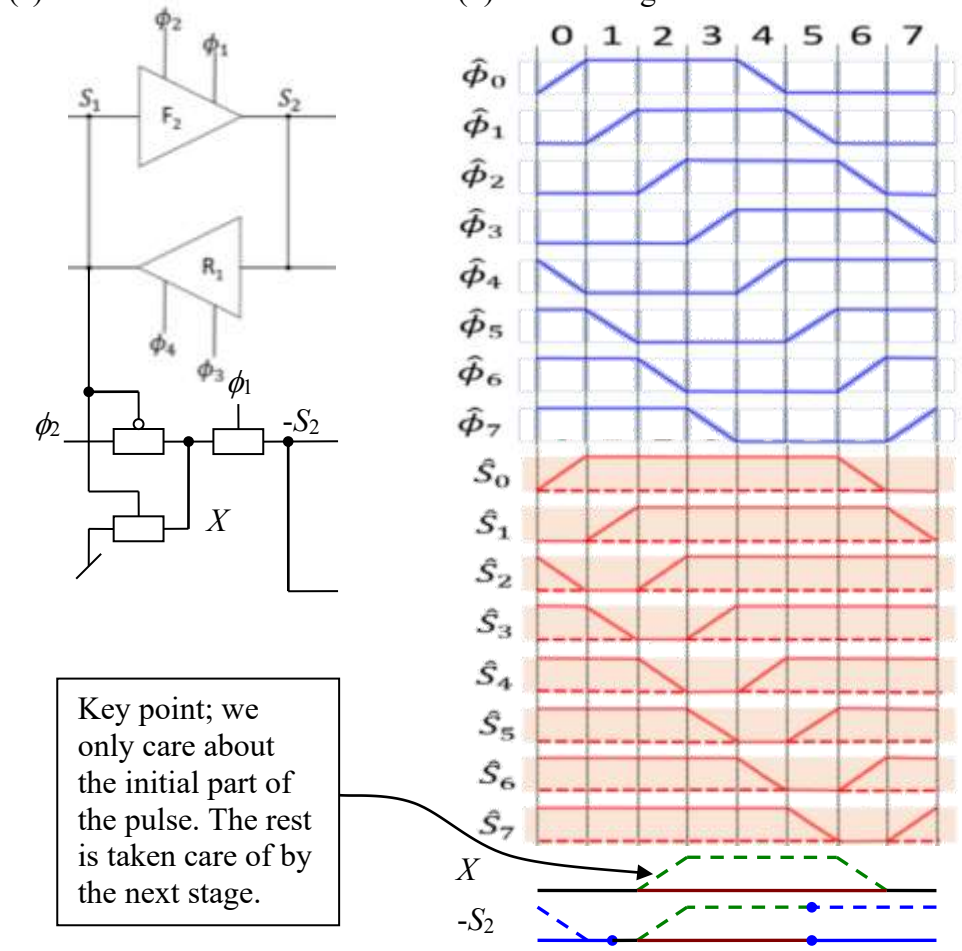

Fig. 1. S2LAL inverter. The (a) base circuit and (b) timing diagrams are copied from ref. 1, but I add three pass gates and the timing to invert the S_2 signal.