Cryogenic Adiabatic Transistor Circuits (CATC) for Quantum Computer Control

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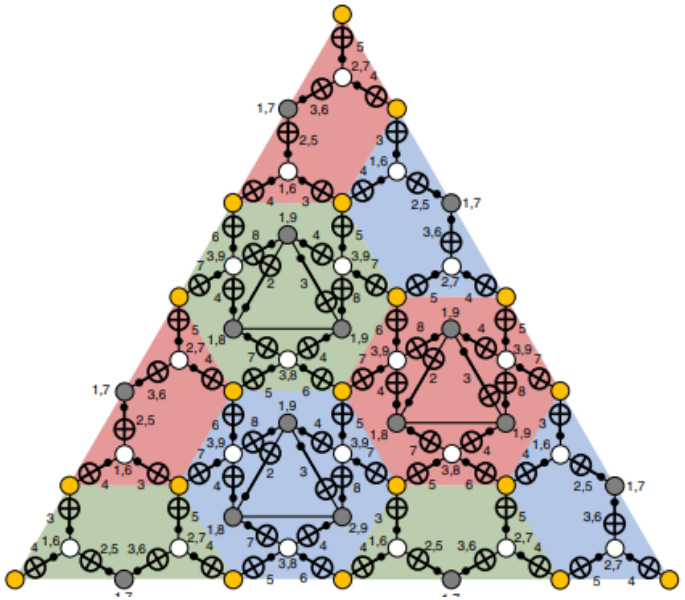
Summary

- Enabling idea:
  - CMOS means (1) transistors and (2) a circuit
  - Let us use the same transistors in a different circuit
- Benefits:
  - ~1/1,000 energy or heat in the cryostat
  - Lower noise in terms of power/amplitude
  - Noise can be below qubit control at frequencies
  - Example cryo FPGA hybrid (e. g. reconfigurable logic)
- See https://zettaflops.org/q2lal
  - Preprint of extended abstract; Q2LAL circuit paper

Use Case: Classical Control of Quantum Computers

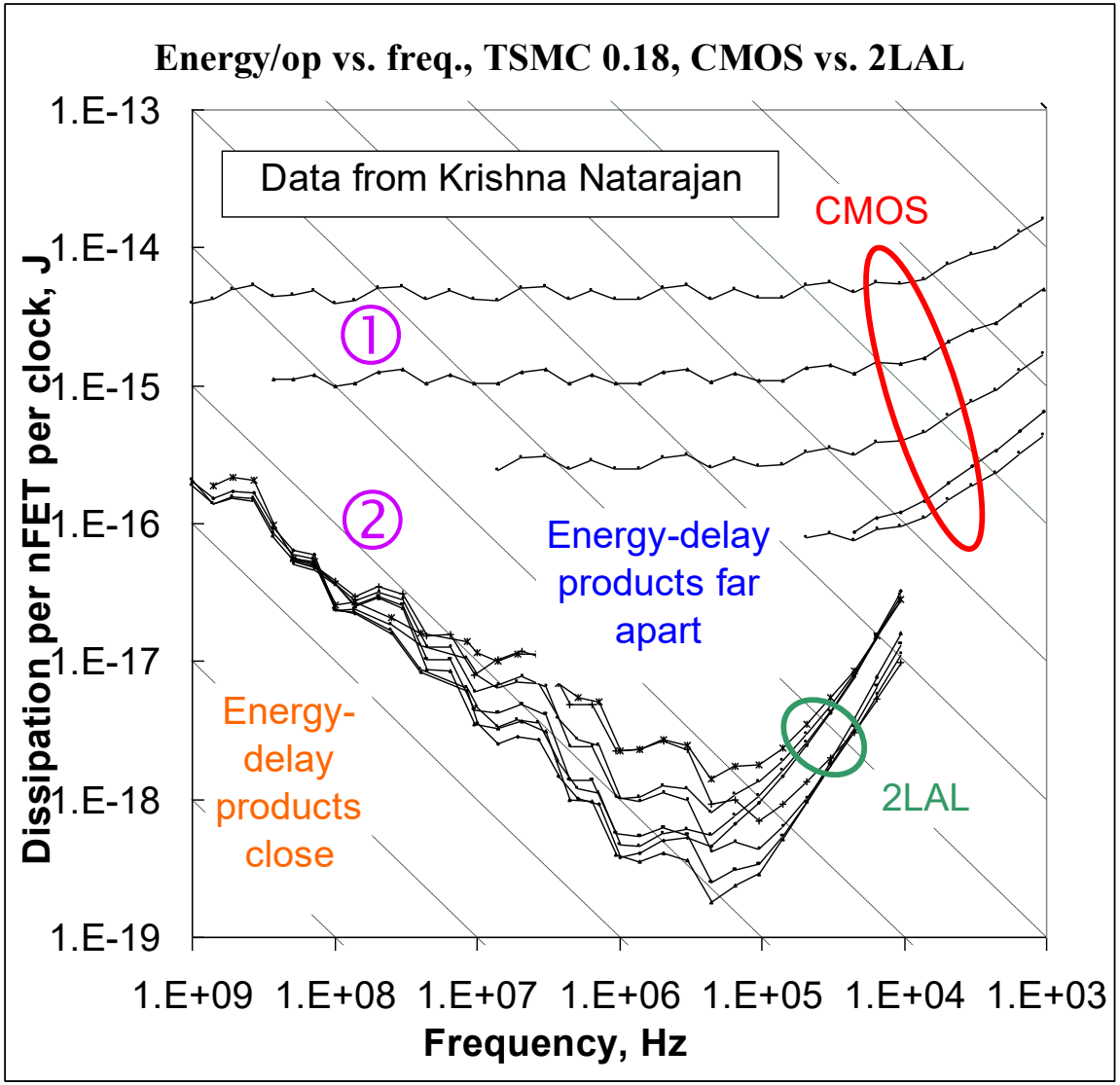
- Some classical function should be near qubits
  - Set to |0> by measure and conditional NOT
  - Quantum error correction
  - Magic state factories
- Example from talk
  - Magic state factory



arXiv:2003.03049

Adiabatic Circuits

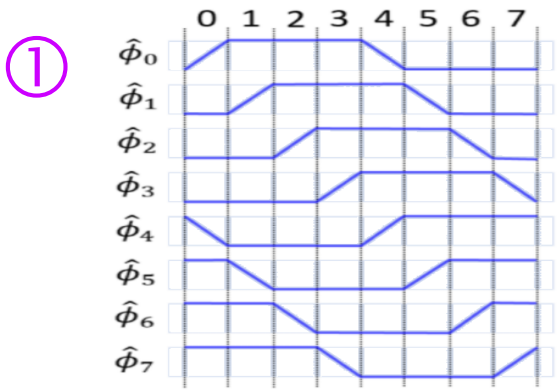
- Energy/op vs. clock period
- CMOS constant energy/op
- Adiabatic energy per op drops with clock period
- 1000× energy efficiency increase reasonable



Quiet 2 Level Adiabatic Logic

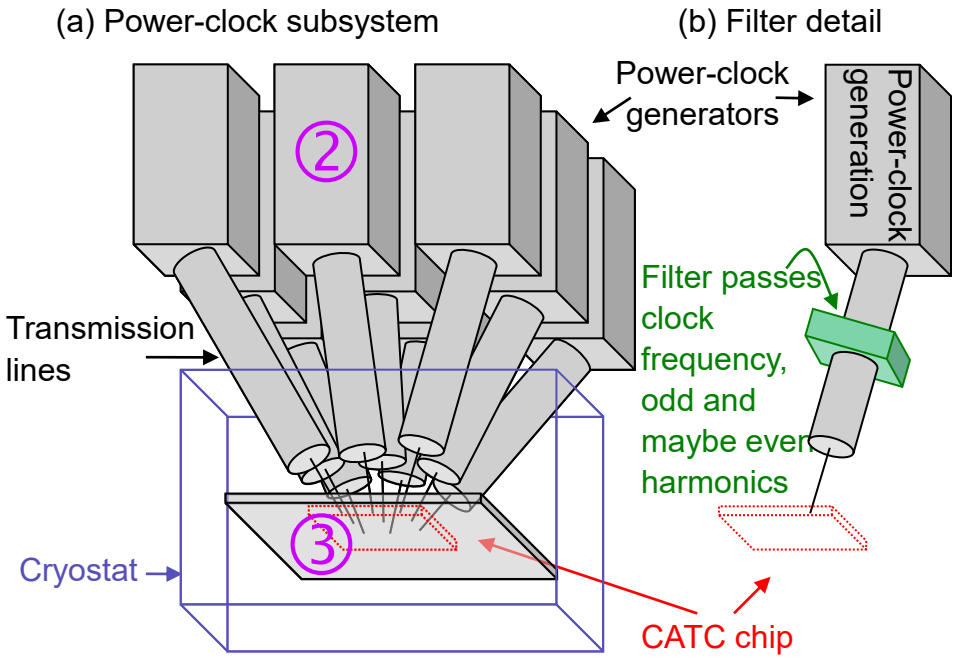
Q2LAL power-clocks

- Ramped power-clocks charge transistors gates
- No abrupt charging



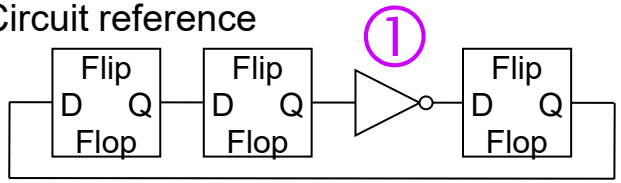
Q2LAL power train

- Power-clocks charge transistor gates) and then leave by reflection

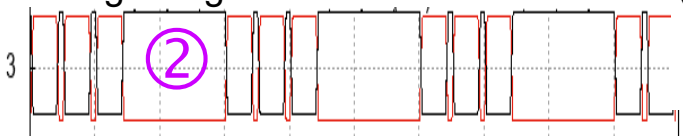


Even-load Adiabatic Logic Family Based on Cyber Security

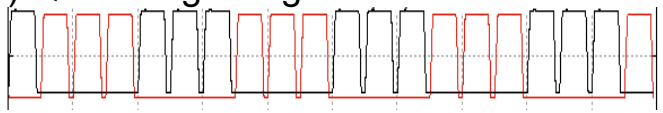
(a) Circuit reference



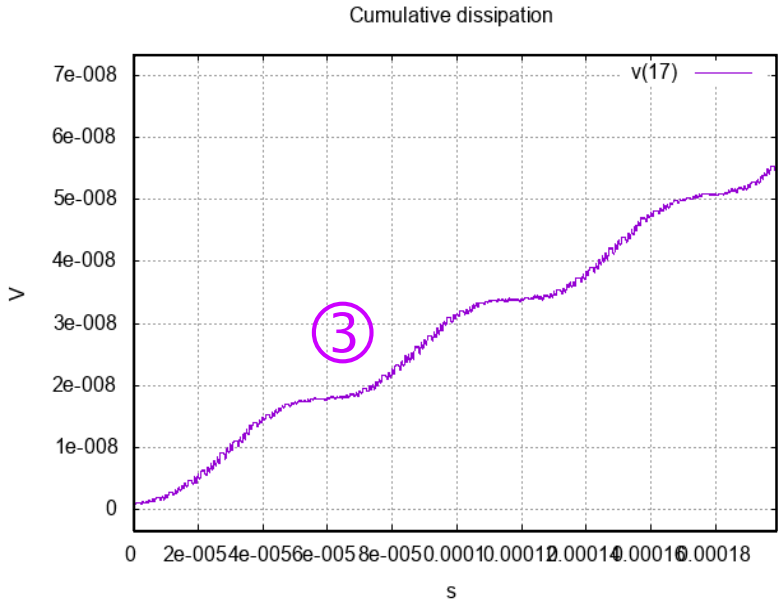
(b) S2LAL signaling



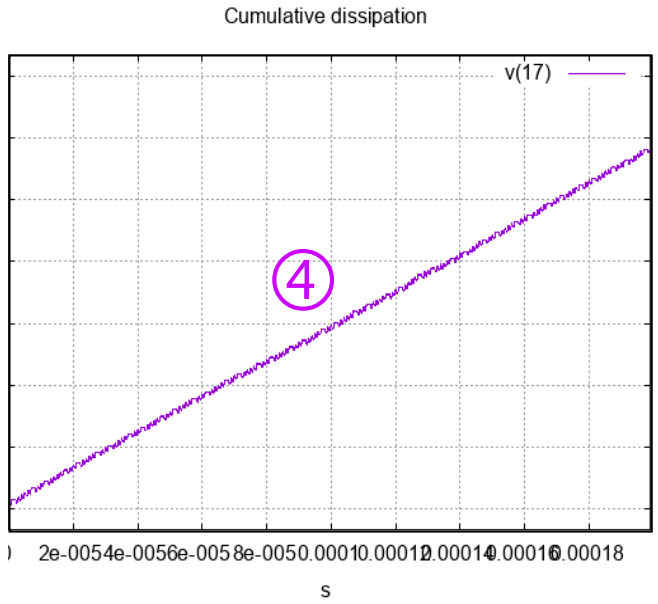
(d) Q2LAL signaling



(c) S2LAL + inverter



(e) Q2LAL + inverter



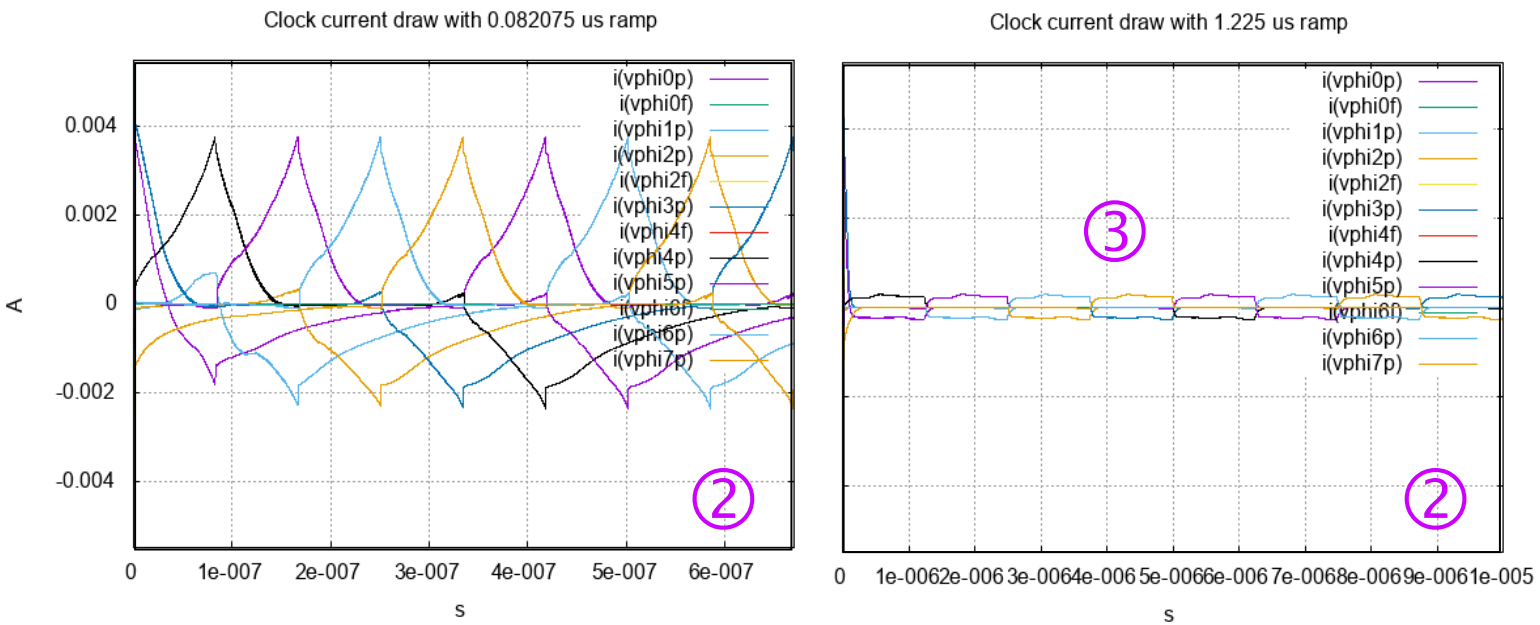
CMOS vs. CATC noise

- CMOS noise from delta functions with frequencies determined by devices

- CATC Noise from clock
- Below same vertical but 15× expanded horizontal scale

(a) Power-clock current at a reference clock period

(b) Power-clock currant at 15× clock period

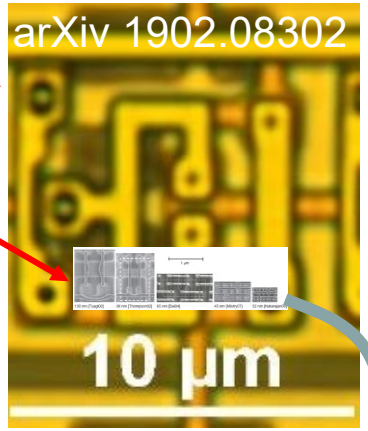


Single Flux Quantum (SFQ) and CATC Hybrid

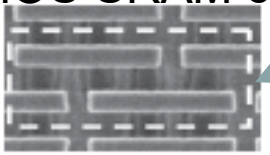
Same scale;
JJs are larger
but very
energy efficient

①

JJ SRAM cell



CMOS SRAM cell



32 nm [Natarajan08]

1 μm

CMOS VLSI Design, Weste

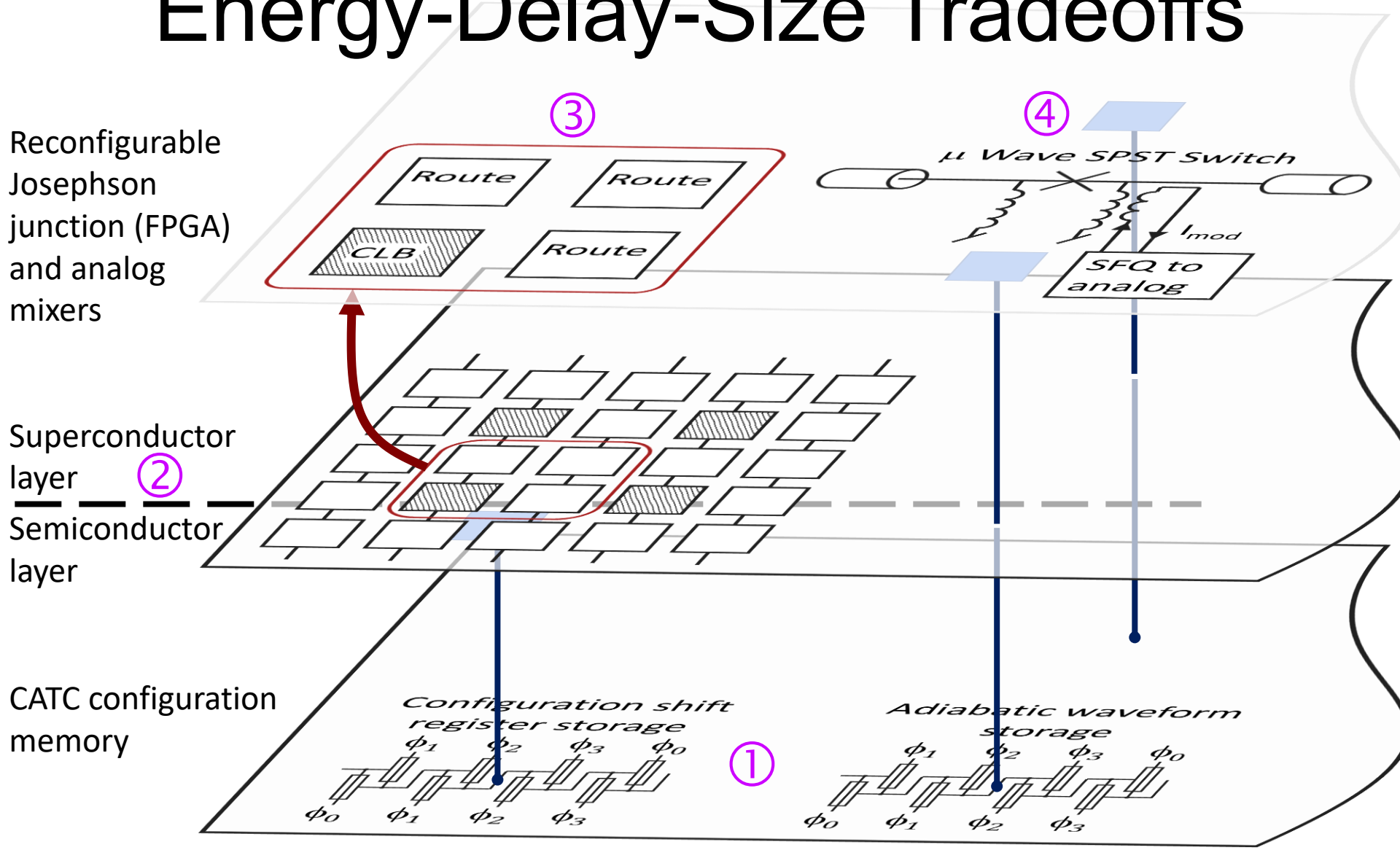
- CATC vs. JJ/SFQ

② – CATC 1000× smaller
– Same energy
– CATC 1000× slower

- Why would you want JJs plus a lot of slow transistors?

③ – Memory
– Complex logic

Transistors/JJ Hybrid Exploits Energy-Delay-Size Tradeoffs



Conclusions

- Adiabatic circuits not new, but use case is new
  - First part of this talk could have been made 30 years ago
  - But the use case didn't exist, i. e. bypass the cryostat
- Benefits today:
  - 99% - 99.9% heat bypasses the refrigerator, permit scaleup
  - Lower noise in terms of power, noise, and bandwidth
- Future
  - Physical demo in quantum control use case
- For more information see https://zettaflops.org/q2lal
  - Preprint of extended abstract; Q2LAL circuit paper