Improving Quantum Computer Scalability with Cryogenic Reversible Logic

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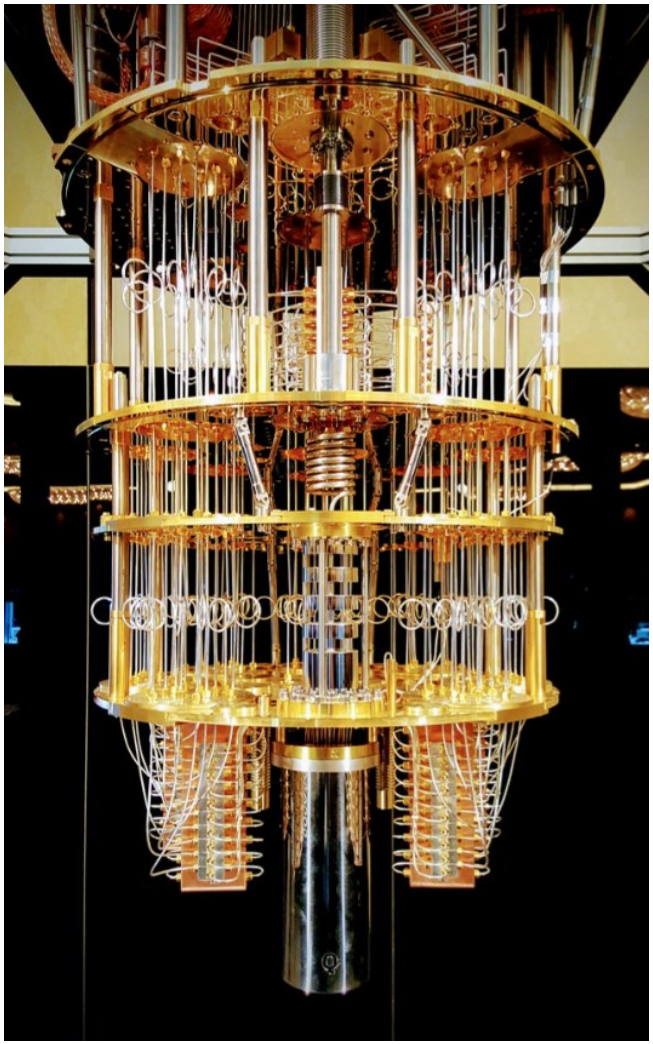
Problem description

- Quantum computers are a national priority
- The structure on the right does not scale
- For cryogenic qubits, the accepted direction is to compress the data in the cables and use cryogenic electronics to decompress
- *De facto* cryo electronics is cryo CMOS at 4 K, which works about the same as 300 K
- CMOS improving at 2×/decade due to fab, which is not enough for the national priority
- Can we do better?
- Photo by Lars Plougmann, https://www.flickr.com/photos/criminalintent/39660636671, license https://creativecommons.org/licenses/by-sa/2.0/

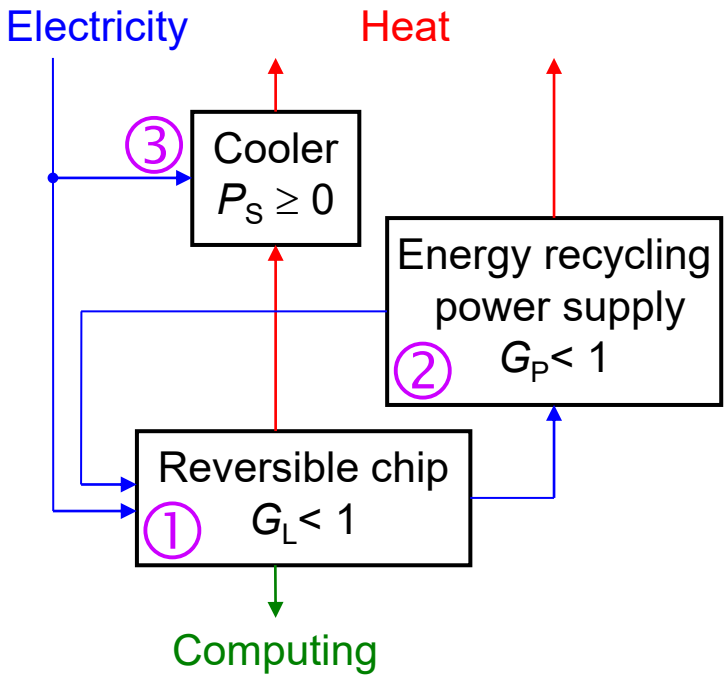


Reversible logic at room temperature and cryo

- Reversible logic discards energy as electricity rather than heat after use. See my previous talks for detail
- Room temperature: recycles energy in loop ① and ②
  - G_P is lower than G_L and limits performance
- Cryogenic: bypass cryocooler and save cryocooler overhead
  - $P_S \approx$ 1,000 at 4 K
- Both concepts work, but cryo lower risk because cryocoolers are COTS

G_P = the energy recycling efficiency of the power supply
G_L = 1 - $2RC/\tau$, the portion energy not turned into heat
P_S = the cooling over head of the cryo cooler, or 0 if not present

- Energy/heat flow diagram

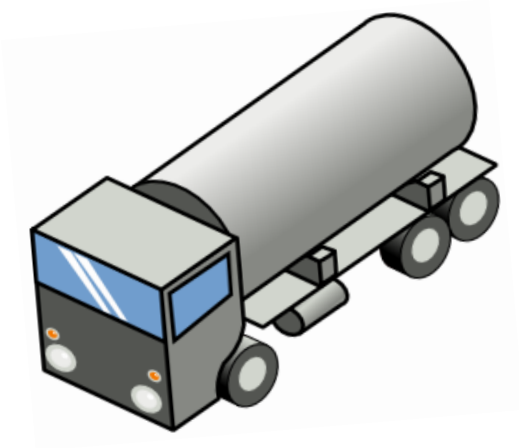


How could reversible logic impact industry plans?

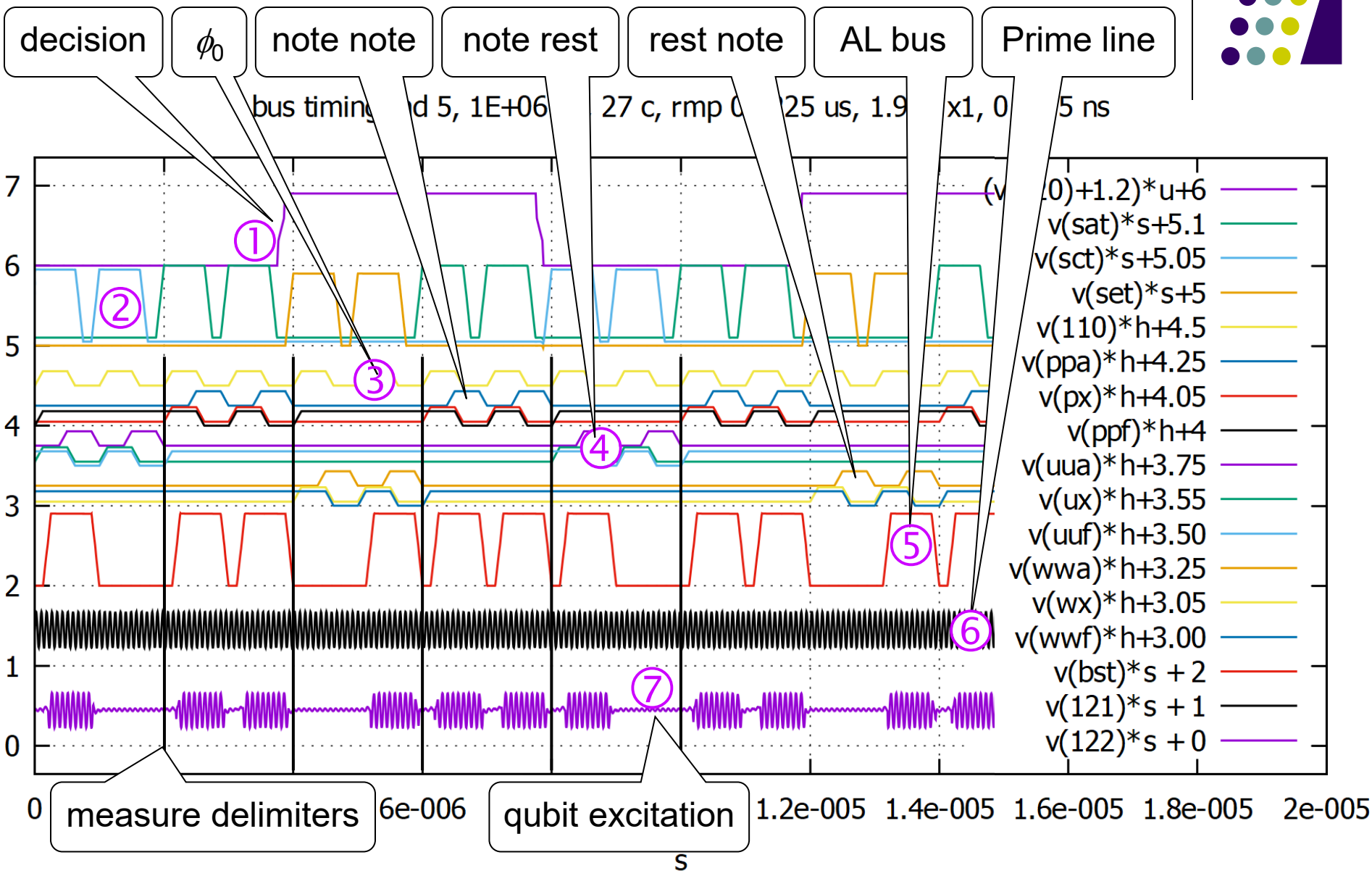
- Diagram from a major player projecting a million-qubit quantum computer. Looks like 10 m of submarine hull
- Lower dissipation control electronics should reduce heat, cooling capacity, and congestion, allowing more qubits per unit volume and cost
- Could the same number of qubits be possible in a structure the size of a tank truck?

See 26 mins 1 sec into the youtube https://www.youtube.com/watch?v=mmyq1ubjqO8

Anthony Megrant, Google,
Quantum Week 2021 keynote



PL/AL architecture & note note



Summary: algorithm-flowchart-schematic then fab

- Error correction procedure

1. Use the circuit of Fig. 2(c) to extract the *XZZXI* syndrome. ①

   (a) If the flag qubit is measured as |->, then use the unflagged circuits analogous to Fig. 2(b) to extract all four syndromes. Finish by applying the corresponding correction from among *IIIII*, *IIZXI*, *IXZXI*,*IYZXI*, *IZZXI*, *IIIXI*, *IIXXI*, *IIYXI*.

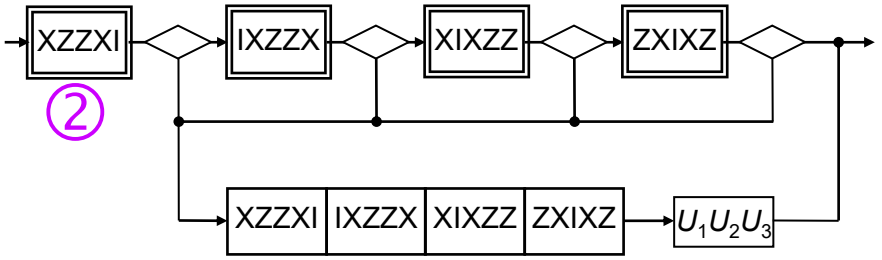
   (b) Otherwise, if the syndrome is −1, i.e., the syndrome qubit is measured as |1>, then use unflagged circuits to extract all four syndromes. Finish by applying the corresponding correction of weight ≤ 1.

2. (If the flag was not raised and the syndrome was trivial, then) Similarly extract the IXZZX syndrome. If the flag is raised, then use unflagged circuits to extract the four syndromes, and finish by applying the correction from among *IIIII*, *IIIIX*, *IXXII*, *IIIXX*, *XIIIY*, *IXIII*, *IIIZX*, *IIIYX*…

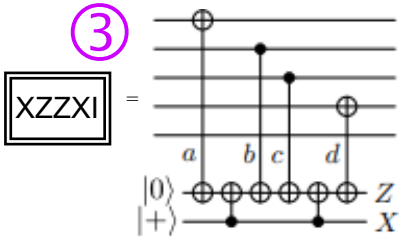
From: Chao, Rui, et. al "Quantum error correction with only two extra qubits." Physical review letters 121.5 (2018): 050502.

- Create "flowchart"

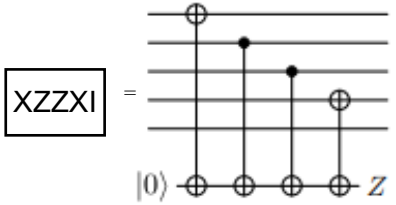
[[5, 1, 3]] error detection and correction with flags:



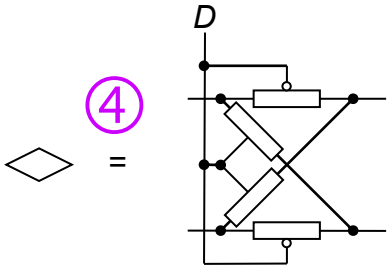
Circuit with flag qubits:



Circuit without flags:



Decision, implemented by a crossover:

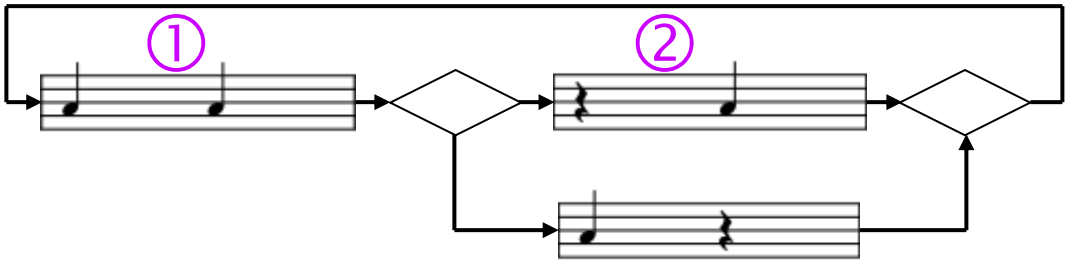


Correction:

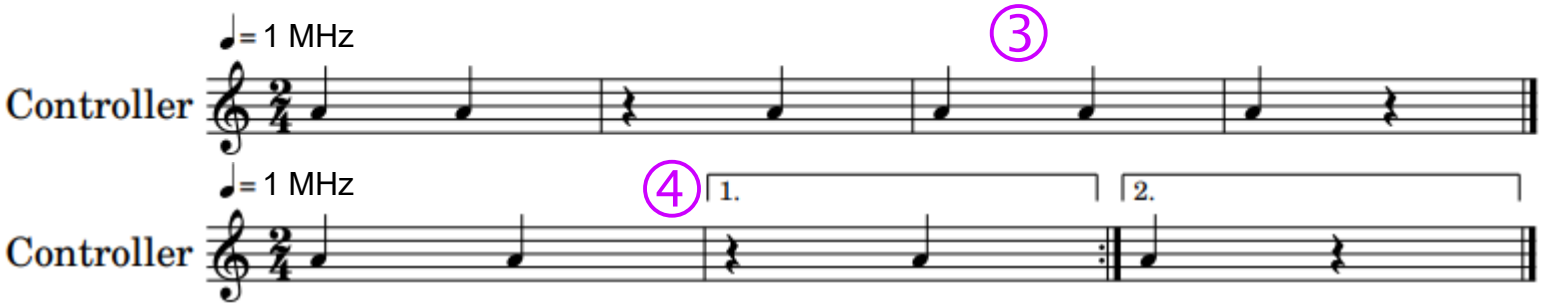
$U_1U_2U_3$ = Z, Y, or Z on qubit *n*

Note note abstraction and potential test chip

- Flowchart

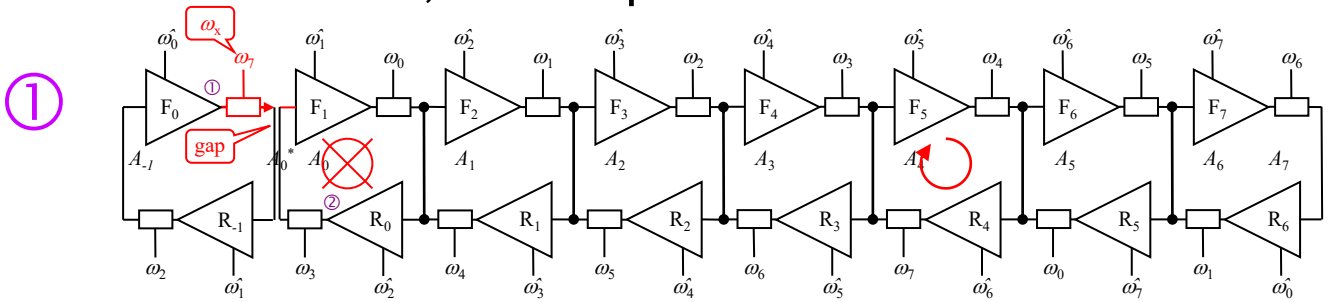


- Musical equivalent

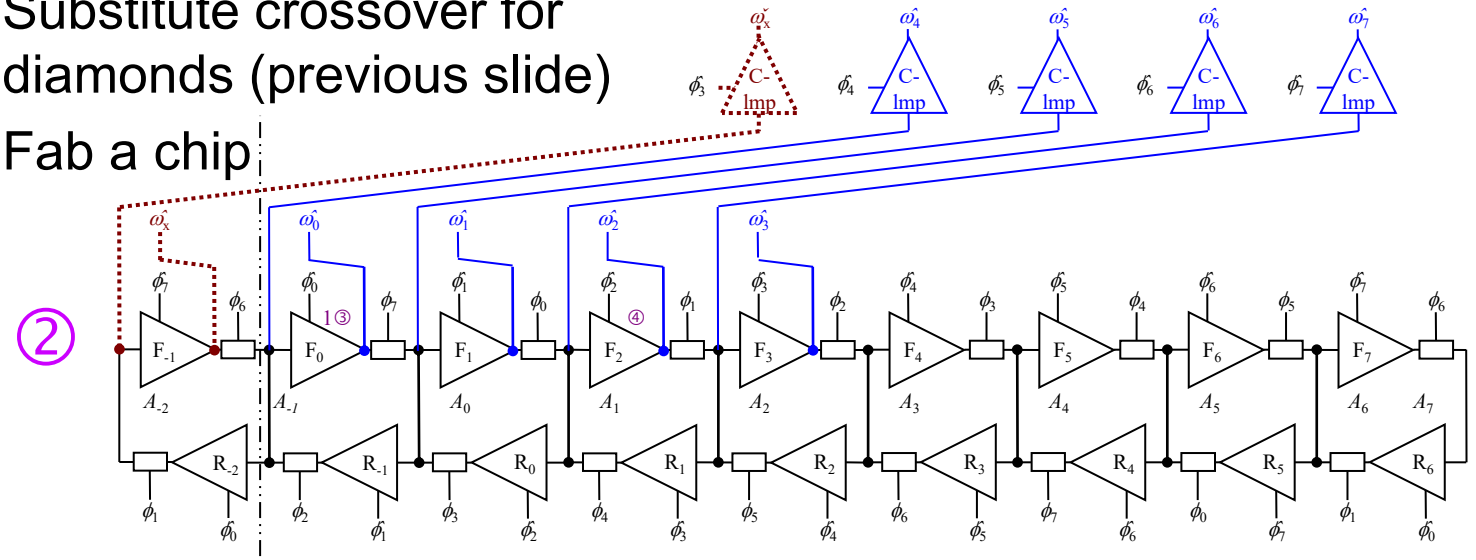


Substitute circuits for boxes and diamonds; keep wires; fab

- Substitute these circuits, but keep flowchart interconnect as wires

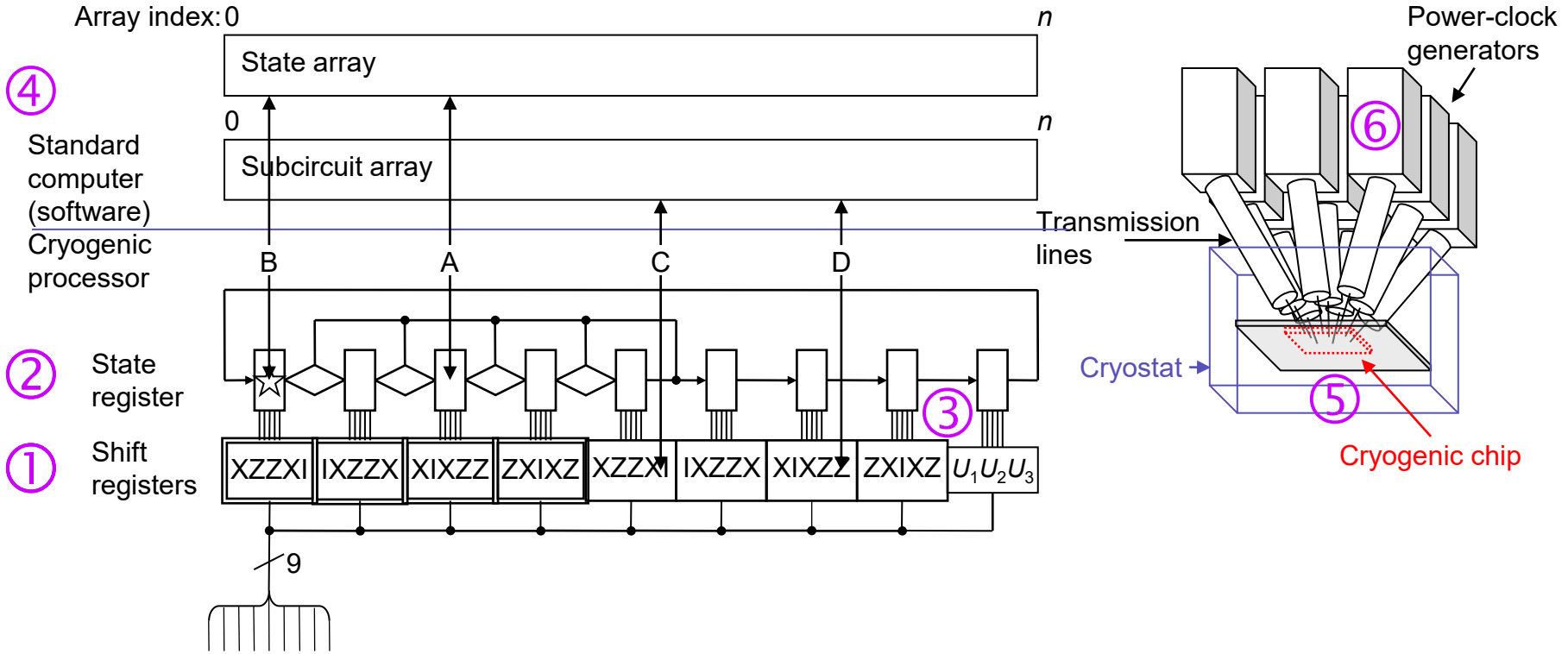


- Substitute crossover for diamonds (previous slide)
- Fab a chip



Hybrid computing system

- Yields an integrated multi-temperature computing system
  - Function
  - Powertrain
- Only reversible shift registers at cryo stage
- If you think about it, cryo stage is a zip/gif decompressor



Results of Simulation

- ngspice Sky130; CMOS from standard cell
  - R_{FOM} 1 MHz 131 @ 27 C
  - Note: Other orgs chips include an instruction set, raising dissipation
- Simulation output:

```
*** OVERALL ADIABATIC ADVANTAGE
* override J_S in q2.cir to use full circuit and make sure .includes are q2.cir and ar.cir
*.param MD=5 J_S=2 Vp=1.9V     Hz=1e6      T=27   wX=1  ww=500e-9   ll=150e-9   Cw=.01p     Cb=0        xl=1.9      xn=1  xh=1.9      yl=1e6      yn=1  yh=1e6
* 0 Adia , 5 , 7.44291E-13 , Ecyc , 5.92981E-14 , Vp , 1.9 , tw , 1E+06 , Vx , 1.9 , 0.625 , 1E-14 , 27 , 1 , 1 , 960.726
*.param MD=5 J_S=2 Vp=2.15V    Hz=1e6      T=-55  wX=1  ww=500e-9   ll=150e-9
* 0 Adia , 5 , 9.25436E-13 , Ecyc , 5.35942E-14 , Vp , 2.15 , tw , 1E+06 , V
* now switch .includes to c2.cir and cr.cir
*.param MD=5 J_S=2 Vp=1.8V     Hz=1e6      T=27   wX=1  ww=500e-9   ll=150e-
* 0 CMOS , 5 , 7.8273E-12 , Ecyc , 7.77908E-12 , Vp , 1.8 , tw , 1E+06 , Vx
*.param MD=5 J_S=2 Vp=1.8V     Hz=1e6      T=-55  wX=1  ww=500e-9   ll=150e-
* 0 CMOS , 5 , 2.40974E-12 , Ecyc , 2.39103E-12 , Vp , 1.8 , tw , 1E+06 , V
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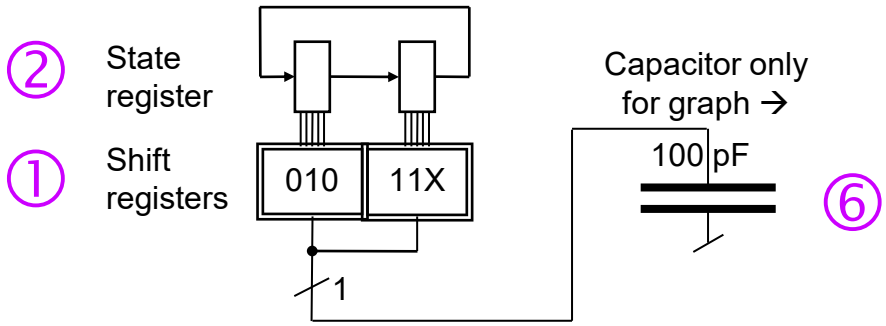
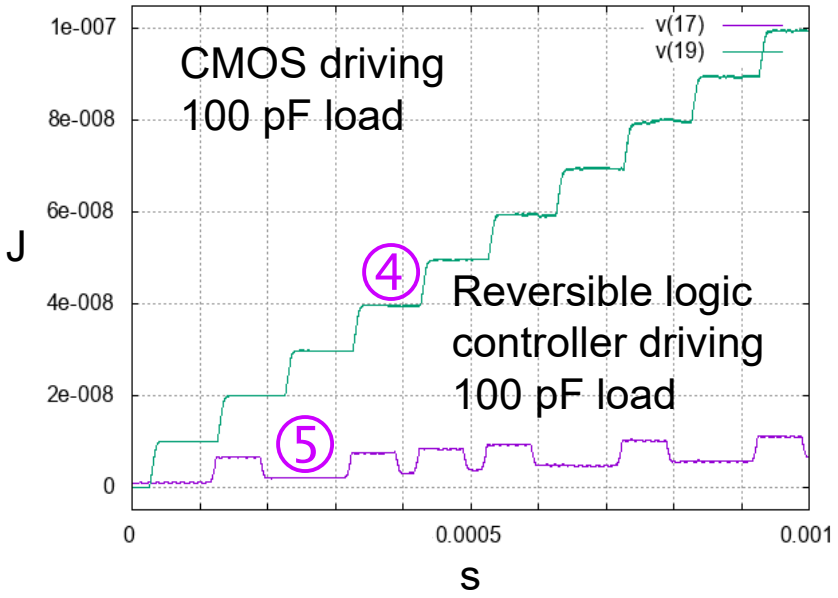
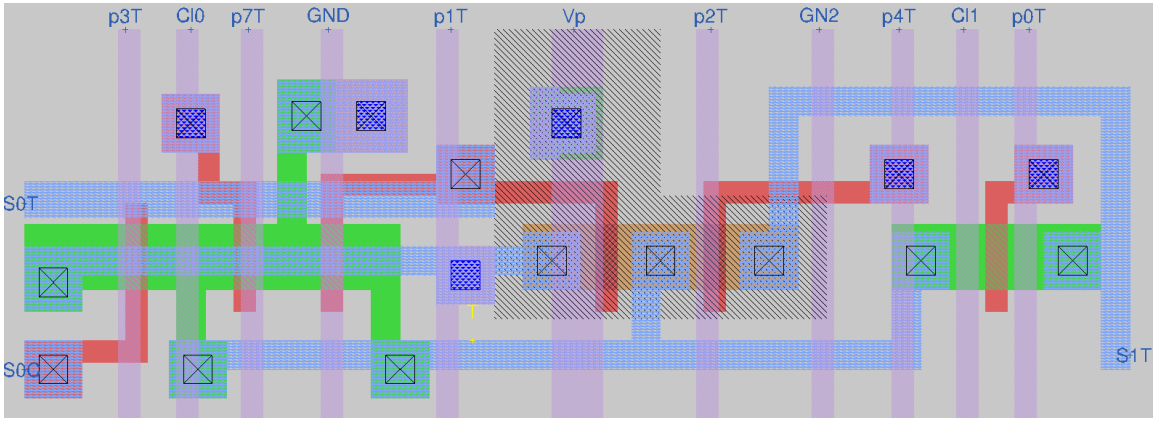




Sky130 validation

- Sky130 is an “open” PDK for multi-project wafers, based on a 130 nm process (I have no cryo data)
- Activity
  - “Note note” has been hand-coded in ngspice and various simulation results have been presented at conferences
  - The replicable unit of Q2LAL (circuit family) is shown below. It has been extracted with parsitics and can be incrementally substituted into the hand-coded ngspice
  - Results are in line with predictions
    - 131× advantage over Cryo CMOS from Sky130 standard cells



Computing in a hybrid mixed temperature environment

Physicist vs. computer architect

- Landauer's minimum is kT per irreversible operation
- In a mixed temperature environment, which T do we use?
- Physicist's answer: The T of the environment performing the function
- Computer architect's answer: What are the limits of moving the irreversible operations to an environment where T is most favorable?

Erik's candidate architecture

- Room temperature:
  - Compute the answer
  - Compress the answer
- Cable:
  - Move data across the temperature gradient
- Cryo electronics:
  - Decompress the answer
- Erik's solution
  - Cryogenic environment only has reversible components (shift registers, crossovers)

Conclusions

- Moore's law may continue for cryo electronics for quantum computers – but not classical computers
  - By continue I mean 100× ±
  - This will be controversial
- While (room temperature) reversible logic has been stalled for decades, it should be possible to create an initial (cryo reversible) quantum control chip as a development project in (say) one year
- The theoretical framework can be simulated with the Spice circuit simulator (achieving 131×) and future work has been proposed for test chips driving qubits
- This talk provides a theoretical framework for classical control overhead based on physics of computation (Landauer's minimum)