A Memory Option for Quantum Computer Control:
Cryogenic Adiabatic Transistor Circuits

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Overview

- Thanks to Joe Glick for the half-hour introduction
- Thanks to Mike Frank for inventing 2LAL circa 2000
- Quantum computer scale up creates a new demand for cold, <u>scalable</u> electronics
- Driver: Cryo adiabatic transistor circuits
  - Eject waste energy to room temperature electrically
- Applies to quantum computer control
  - Provides a memory to complement JJs
  - Narrow applicability; won't apply to Exascale
  - Applies to transmons, quantum dot, ion traps
  - Should work at 4 K today; will it work at mK?

Comparison to competition

- Paper (TAS early access)

- This approach 30,000× more efficient for trans

Design and demonstration of an
adiabatic-quantum-flux-parametron
field-programmable gate array using
Josephson-CMOS hybrid memories

Yukihiro Okuma, Naoki Takeuchi, Yuki Yamanashi, *Member, IEEE* and Nobuyuki Yoshikawa, *Senior Member, IEEE*
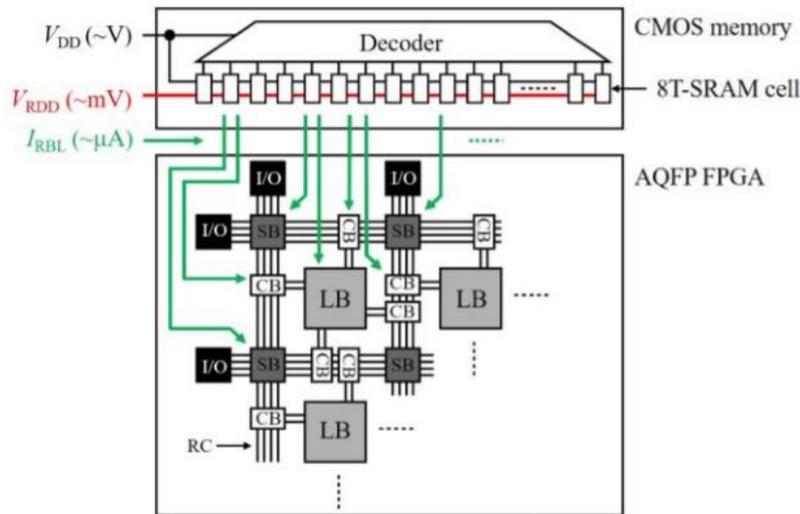

Fig. 1 Conceptual diagram of an AQFP-CMOS hybrid FPGA using a Josephson-CMOS hybrid memory.

TABLE II
Junction number, circuit area, memory cell number, power consumption of AQFP-CMOS hybrid FPGAs with two-by-two and 32-by-32 logic cells.

	2×2 logic cell system	32×32 logic cell system
Junction number of AQFP FPGA circuits	1680	313220
Area of AQFP FPGA circuits [μm²]	1960×3350	36085×44600
Number of CMOS memory cells	68	12548
Power consumption of AQFP FPGA circuits [nW]	12.4	2348
Power consumption of CMOS memories [μW]	1.02	188

	JJ	Transistor
Devices	313,220	75,288
Power	2.35E-06	1.88E-04
Power/Dev	7.50E-12	2.50E-09
Power Ratio	1.00	333.11
CATC-JJ	100	1
Advantage	33,311	

Scalable $(f_{300} \circ f_4 \circ f_{0.015} \circ q)(N)$

Temp	Logic options	Memory-like options	Power	Data processing	Cooling
300 K	CMOS	SRAM DRAM Flash		Stage 1: f_{300}	
4 K 1,000$\times$ overhead	Cryo CMOS JJ SFQ Adiabatic transistor	Excellent progress Adiabatic transistor		Stage 2: f_4 Memory-like Mostly logic	
15 mK 10^6-$10^9\times$ overhead	JJ SFQ Passives Adiabatic transistor ??	Adiabatic transistor ??		Stage 3: $f_{0.015}$ Payload: $q(N)$	
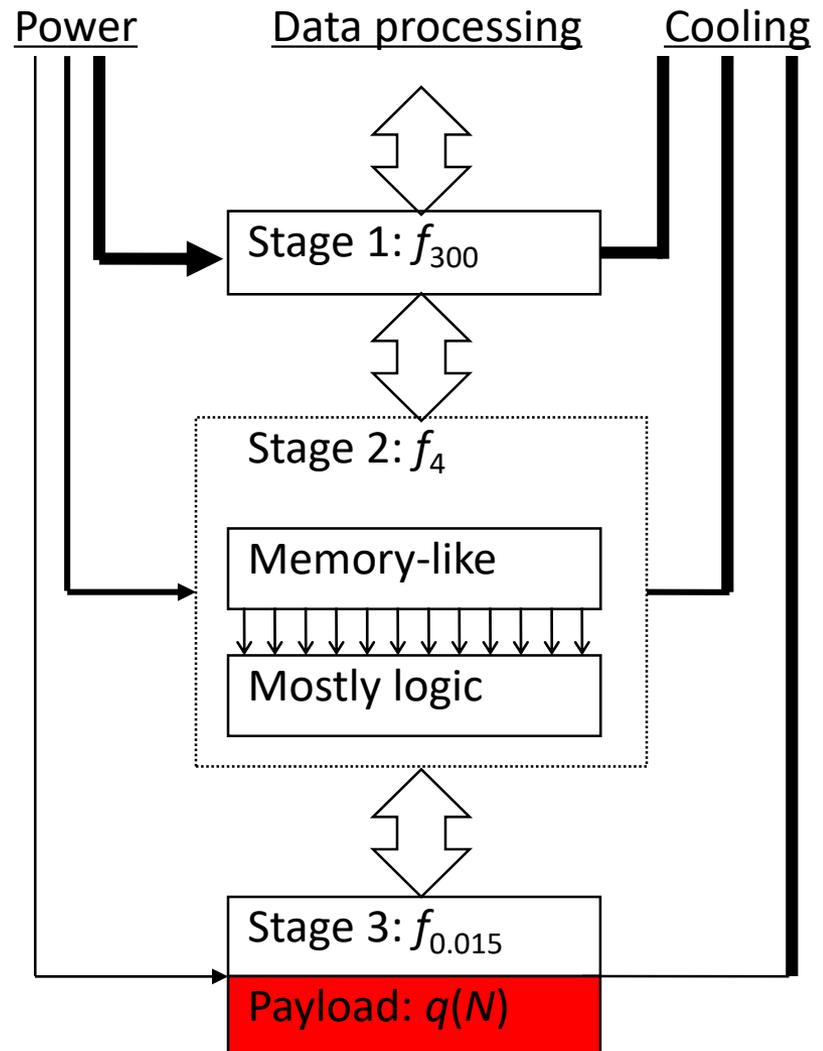
Where does the energy go? I

- All transistor circuits have $\frac{1}{2}CV^2$ signal energy
- Adiabatic 2LAL dissipates less in the chip
- How is that possible given conservation of energy?

Energy/op vs. freq., TSMC 0.18, CMOS vs. 2LAL
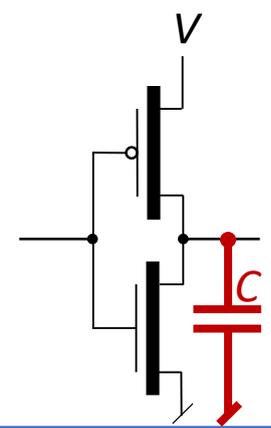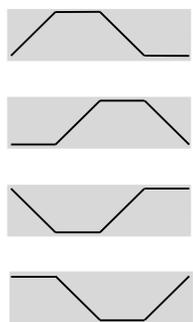
Power/device vs. freq., TSMC 0.18, CMOS vs. 2LAL

Where does the energy go? II

ϕ_0

ϕ_1

$\phi_2 = -\phi_0$

$\phi_3 = -\phi_1$

300 K

Cryo

Energy to switch:

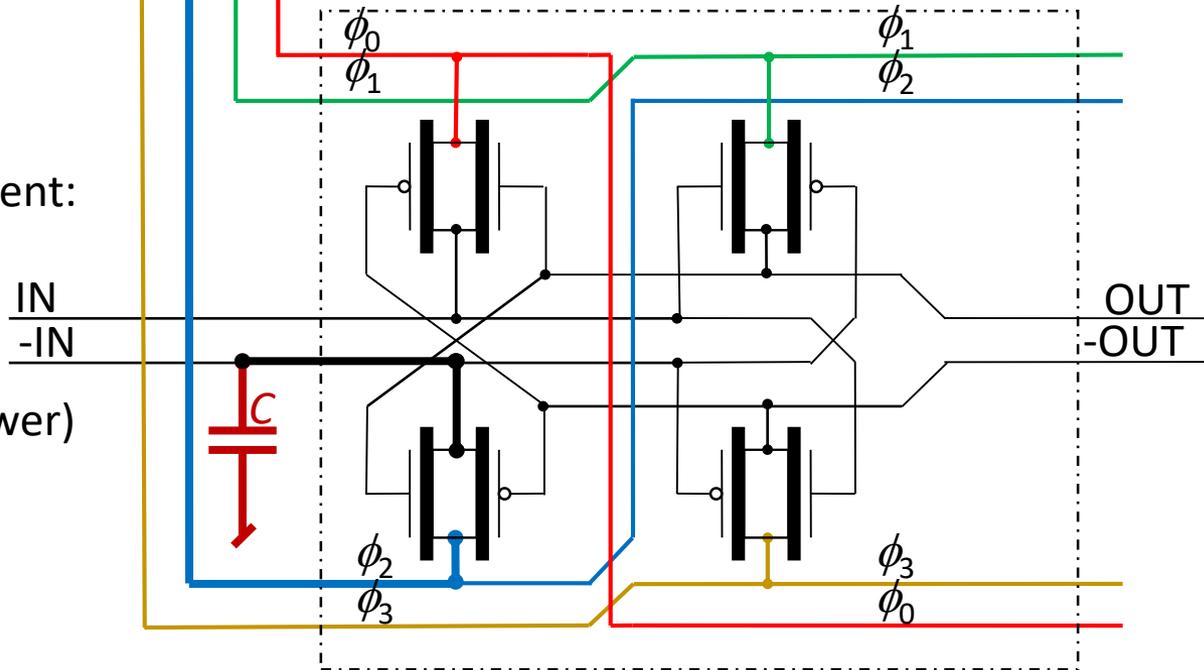$E = \frac{1}{2} CV^2$

AC power supply current:

$I = C\, dV/dt$

Transistor power:

$I^2 R$

Slope -1 (or -2 for power)

Where does it go?

Climbs up the power supply wire to 300 K; then turns in to heat

V
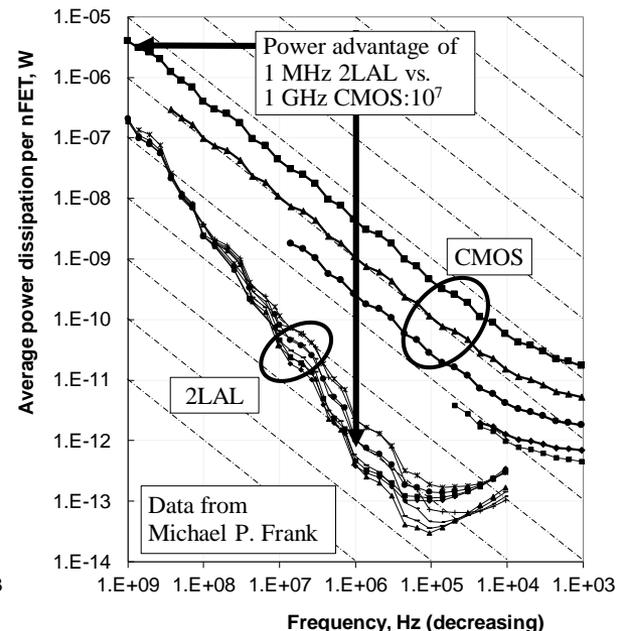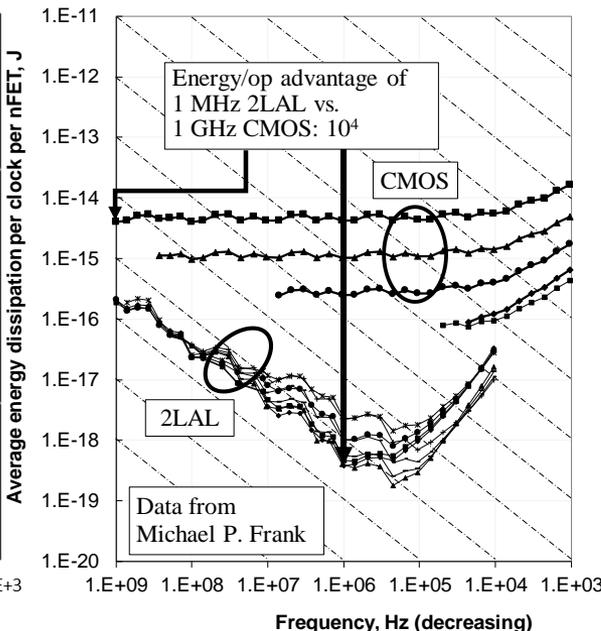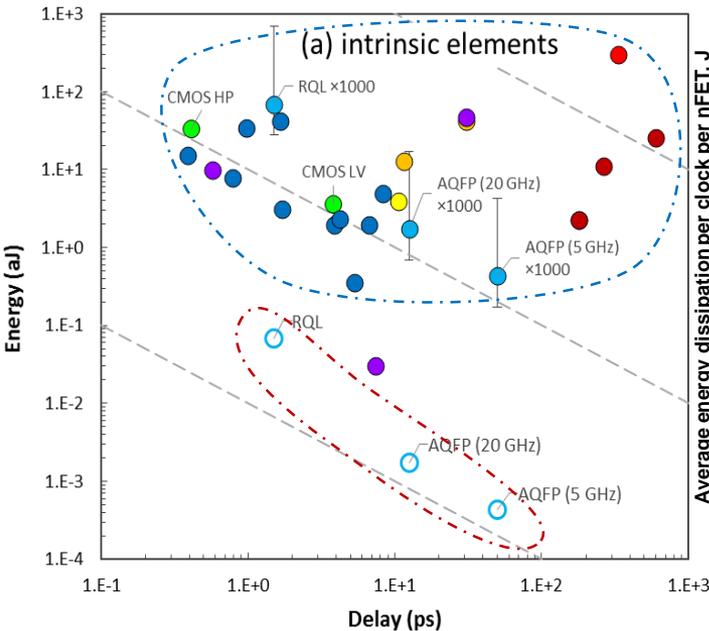
Energy to switch:

$\frac{1}{2} CV^2$

Power to switch at frequency f:

$\frac{1}{2} CV^2 f$

Slope 0 (or -1 for power)

C

ϕ_0
ϕ_1

ϕ_1
ϕ_2

IN

-IN

C

ϕ_2
ϕ_3

ϕ_3
ϕ_0

OUT

-OUT

Mike at Kevin's meeting in 2012

Kevin organized the meeting;
keeps pdfs on personal website

https://www.physics.umd.edu/~kosborn/index_files/SEALeR/Frank-SEALeR-talk.pdf

Adiabatic scaling and hybrids

Power/device vs. freq., TSMC 0.18, CMOS vs. 2LAL
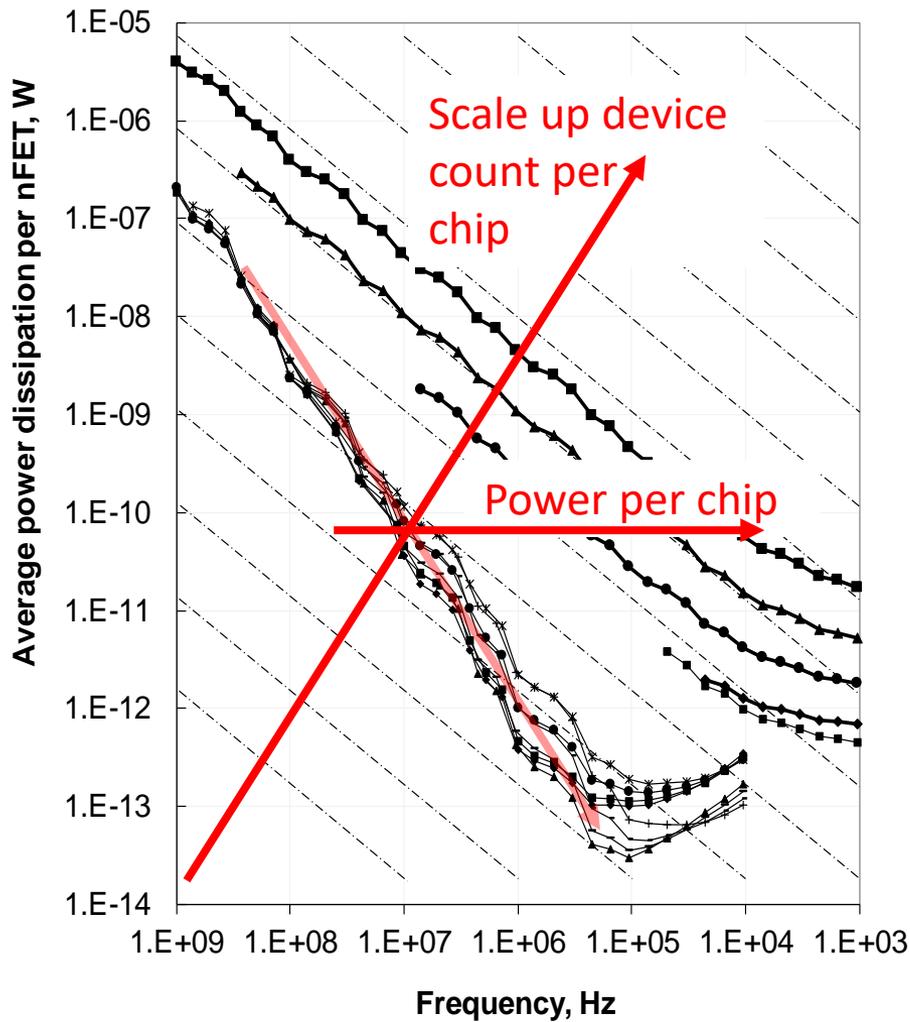
- Scale up clock period – i. e. slow the clock

- Per-gate dissipation drops quadratically

- But add quadratically more devices at same total power

- Will a scalable quantity of slow transistor help current applications?

Question of the hour

- Can cryogenic adiabatic transistor circuits become the memory counterpart for JJ/SFQ?

- If we follow adiabatic scaling, will …
  - device count rise enough to comprise a "memory"
  - before speed makes it unusably slow?

Hybrid technology model

Baseline

1 million RQL gates
1.6 GHz clk, 160 μW at 4 K

Scaling step 3

1 million RQL gates
1.6 GHz clk, 160 μW at 4 K
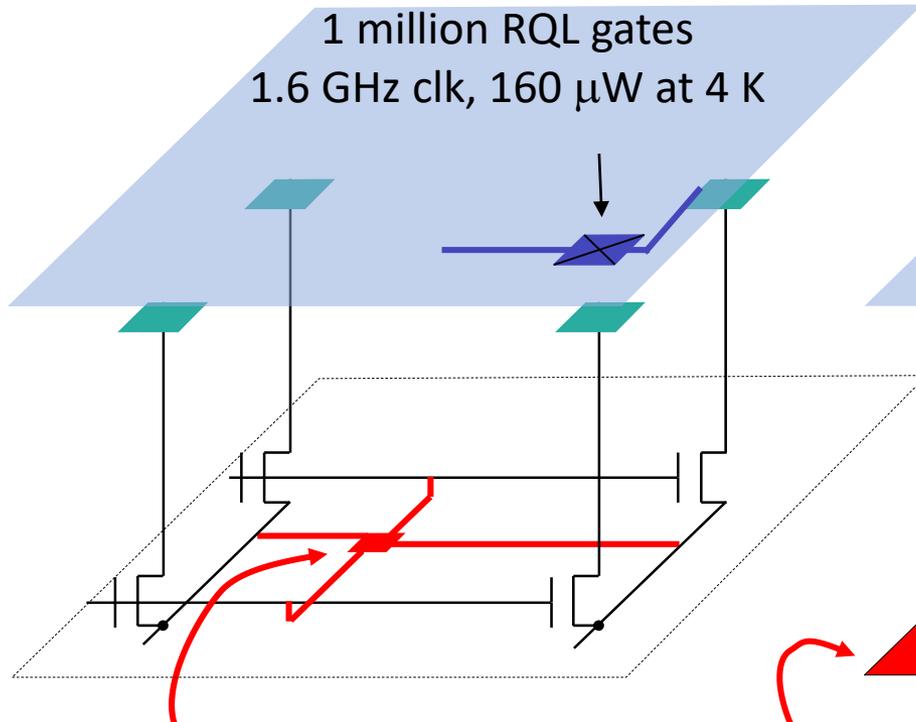
1,000 cryo CMOS gates (to scale)
4 GHz clk, 160 μW at 4 K
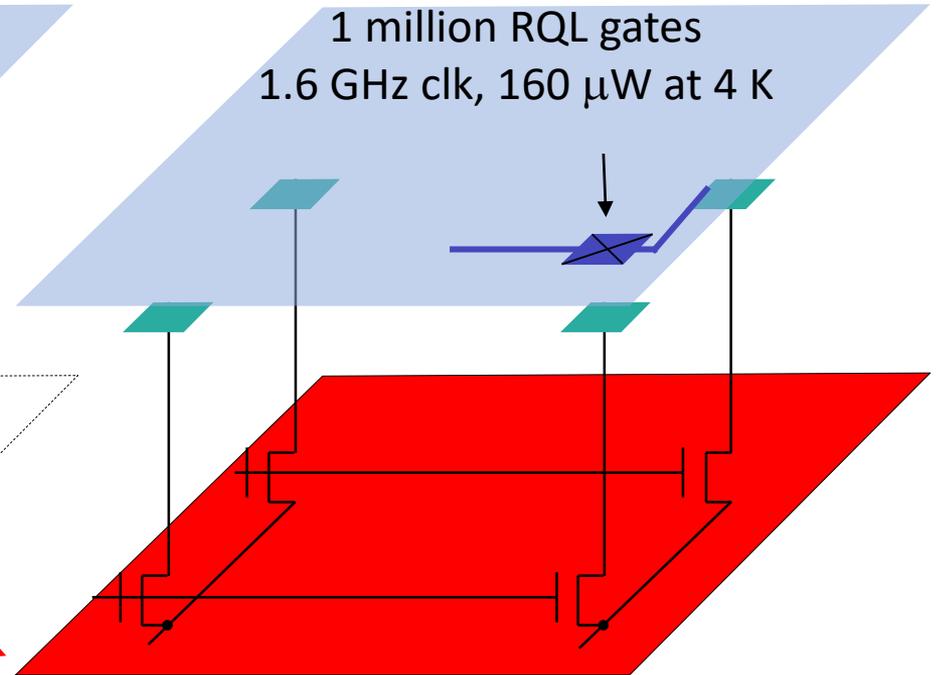
100 million 2LAL gates (to scale)
4 MHz clk, 160 μW + 167 μW (leakage) at 4 K

Backup: JJ-2LAL scaling steps I

- Each step: 100× gates; 1/10 clock rate; same chip power; static leakage rises with device count
- First step CMOS → 2LAL 10× device penalty

Baseline	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 μW	P_{Static} = n/a
	N_{CMOS} = 1 K	f_{CMOS} = 4 GHz	P_{CMOS} = 160 μW	P_{Static} = n/a
Scaling Step 1	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 μW	P_{Static} = n/a
	$N^{(1)}_{2LAL}$ = 10 K	$f^{(1)}_{2LAL}$ = 400 MHz	$P^{(1)}_{2LAL}$ = 160 μW	$P^{(1)}_{Static}$ = 16.7 nW
Scaling Step 2	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 μW	P_{Static} = n/a
	$N^{(2)}_{2LAL}$ = 1 M	$f^{(2)}_{2LAL}$ = 40 MHz	$P^{(2)}_{2LAL}$ = 160 μW	$P^{(2)}_{Static}$ = 1.67 μW
Scaling Step 3	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 μW	P_{Static} = n/a
	$N^{(3)}_{2LAL}$ = 100 M	$f^{(3)}_{2LAL}$ = 4 MHz	$P^{(3)}_{2LAL}$ = 160 μW	$P^{(3)}_{Static}$ = 167 μW

Backup: JJ-2LAL scaling steps II

- Each step: 100× gates; 1/10 clock rate; same chip power; static leakage rises with device count

- First step CMOS → 2LAL 10× device penalty

Baseline	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 µW	P_{Static} = n/a
	N_{CMOS} = 1 K	f_{CMOS} = 4 GHz	P_{CMOS} = 160 µW	P_{Static} = n/a

Device count rises 10^5

Speed drops 1,000×

Chip is now full; power rises 3×

Scaling Step 3	N_{RQL} = 1 M	f_{RQL} = 1.6 GHz	P_{RQL} = 160 µW	P_{Static} = n/a
	$N^{(3)}_{2LAL}$ = 100 M	$f^{(3)}_{2LAL}$ = 4 MHz	$P^{(3)}_{2LAL}$ = 160 µW	$P^{(3)}_{Static}$ = 167 µW

JJ μwave Components

μwave SPST
switch

- There is a need to control microwaves at cryo
  - Northrop-Grumman, Google (Naaman)
  - Transmon quantum computers, etc.

- However, all current options require control signals from room temperature, limiting scalability

JJ FPGAs proposed

Reconfigurable
Josephson
junction (FPGA)
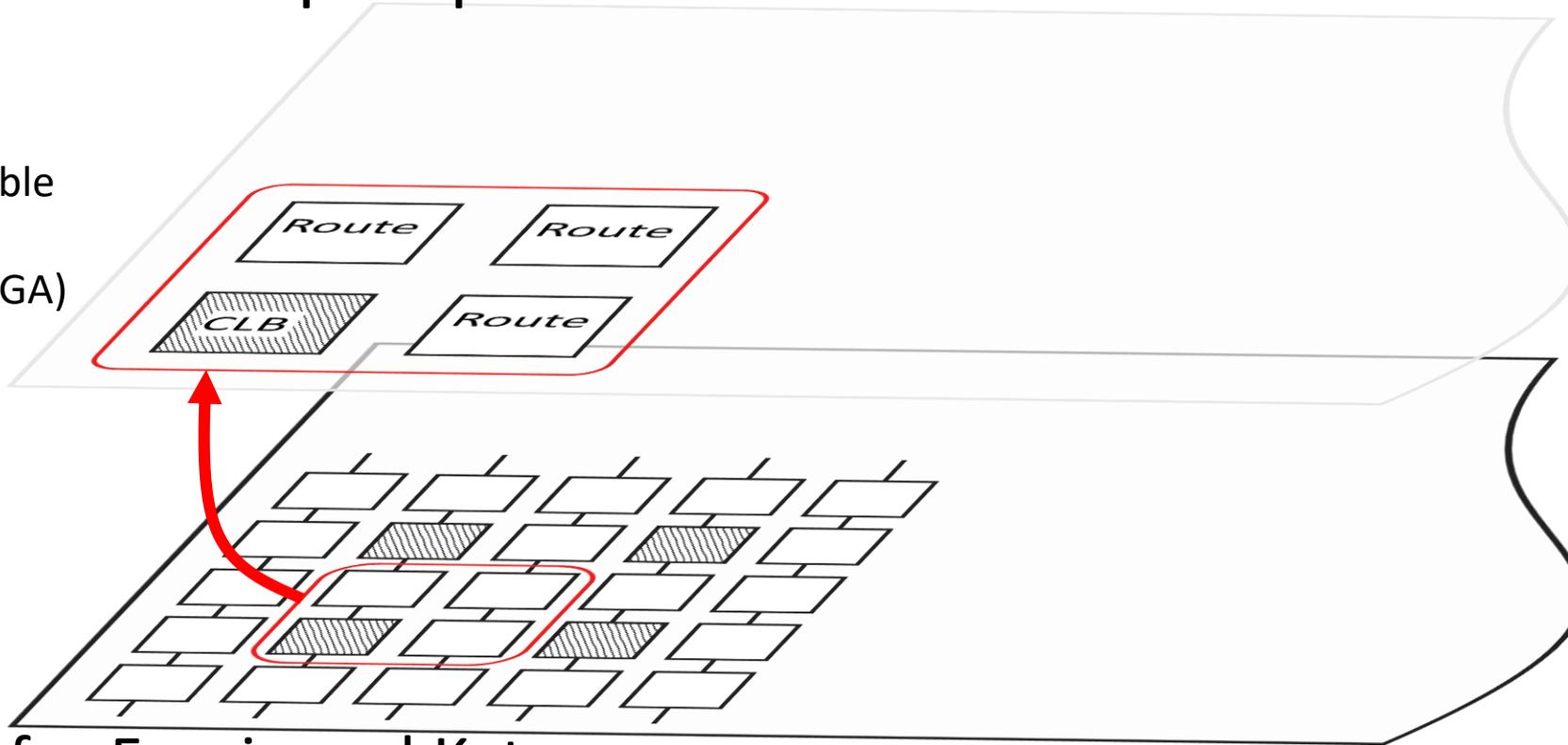
- Refs.: Fourie and Katam

- However, the configuration logic is via JJs, so the result is not very dense

Hybrid 2LAL-JJ controller

Reconfigurable Josephson junction (FPGA)

Route Route

CLB Route

μ Wave SPST Switch

I_{mod}

SFQ to analog
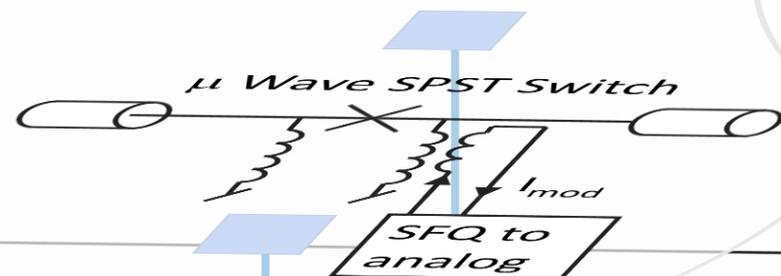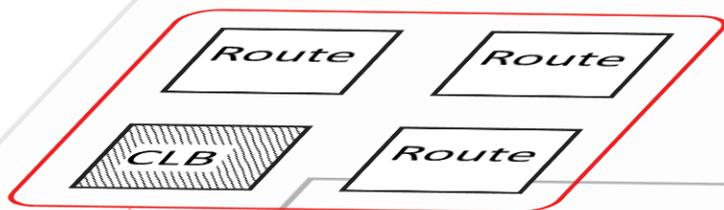
Controlled layer

Configuration layer
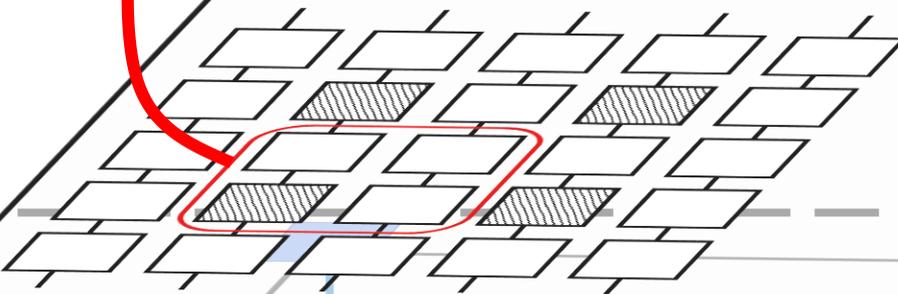
Adiabatic shift register memory

Configuration shift register storage

ϕ_1 ϕ_2 ϕ_3 ϕ_0

ϕ_0 ϕ_1 ϕ_2 ϕ_3

Adiabatic waveform storage

ϕ_1 ϕ_2 ϕ_3 ϕ_0

ϕ_0 ϕ_1 ϕ_2 ϕ_3
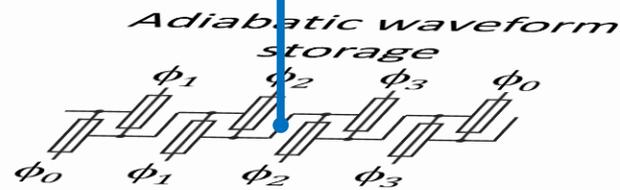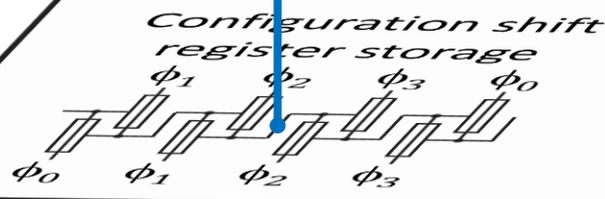
Quantum program with FPGA overlays

Reconfigurable Josephson junction (FPGA)

μ Wave SPST Switch

SFQ to analog

I_{mod}
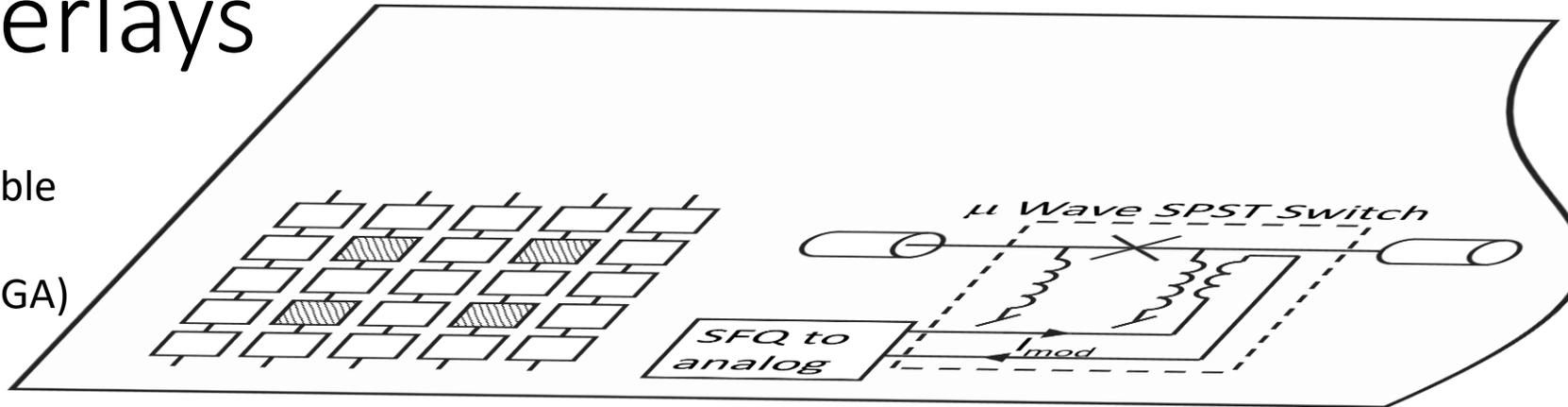
Program via FPGA overlay

Self test
Qubit initialization
Quantum program
Qubit readout
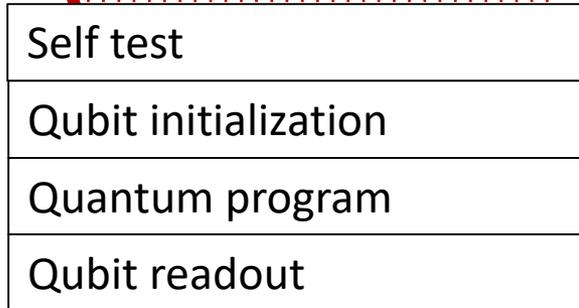
- Reconfiguration time estimate 250 ns

- Qubit decoherence time 10s of μs

- Qubit state can persist across a reconfiguration

Conclusions

- Paper http://debenedictis.org/erik (first link)
- Pre quantum supremacy brings attention to <u>scalable</u> control systems for quantum computes
- Cryogenic adiabatic transistor circuits are helpful due to a principle related to temperature (i. e. "dissipate the heat at 300 K")
- System designers expect a suite of technologies
  - Smartphones need CMOS + DRAM + Flash
  - Cryo systems need JJs + Cryo adiabatic transistor circuits
- Further work:
  - Test hybrid of JJ + 22FFL, 22FDX, 22ULP, or ST 28 FDSOI
  - Test architectures applicable to quantum computer control
  - Rebalance transistors

Backup

Backup: Transistor changes

- Transistors used to experience carrier freeze out and 'kinks,' but natural evolution of transistors means these effects are no longer a problem

- New transistor lines for IoT are on the right path
  - Intel 22FFL, GF 22FDX, TSMC 22ULP, or ST 28 FDSOI

Backup: Basic physics of cooling

- Electric energy is happy to flow through a wire that crosses a temperature gradient in either direction

- Energy in the form of heat flows downhill unassisted, but needs energy to move uphill

- Reversible and adiabatic computing tried to recycle energy with neither uphill nor downhill movement, but the necessary energy-recycling power supply has not been found after looking for decades

- Cryogenic adiabatic transistor circuits move waste across the temperature gradient as energy <u>before</u> turning it into heat, not <u>after</u>

Backup: Transistor properties

- Based on Spice simulations, 4 K quantum computer controllers need to scale 50-72 qubits to the next step should work with Intel 22FFL, GF 22FDX, TSMC 22ULP, ST 28 FDSOI "out of box"

- Custom transistors would help, may not be that different
    - Need ultra-low leakage, i. e. high I_{on}/I_{off} ratio
    - Quantum computer performance comes from the qubits, so the traditional CMOS metrics don't hol
    - Natural steepening of subthreshold slope give maneuvering room; need thicker oxide and threshold adjustment at some point

Backup: Architectural issues

(Cryogenic Adiabatic Transistor Circuit = CATC)

- The CATC advantage is narrow
  - CATCs are slow; need to be a hybrid with something fast to be useful. Fortunately, a CATC-JJ hybrid is natural
  - Memory needs to be dense. Fortunately, CATCs are nearly as dense as transistors, far denser than JJs
  - CATCs are not fast enough to be the addressing logic for RAM, but CATCs work for memory-like structures like shift registers
- FPGAs and buffers
  - Quantum computer controllers are halfway between signal processors and general purpose computers

Backup Cold, scalable controller

- Hybrid FPGA
  - Configured logic: JJs, configuration logic: transistors
  - Problem: JJs are huge
  - Solution: FPGA "timeshares" JJs by on-the-fly reconfiguration
- All-cold SFQ microwave components
  - There is a suite of switches, modulators, etc. available, but they require waveforms piped in from 300 K
  - While we don't know how to make a random access cryo memory, waveforms are accessed as a stream, making the shift register in previous slides sufficient