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# Matching Supercomputing to Progress in Science

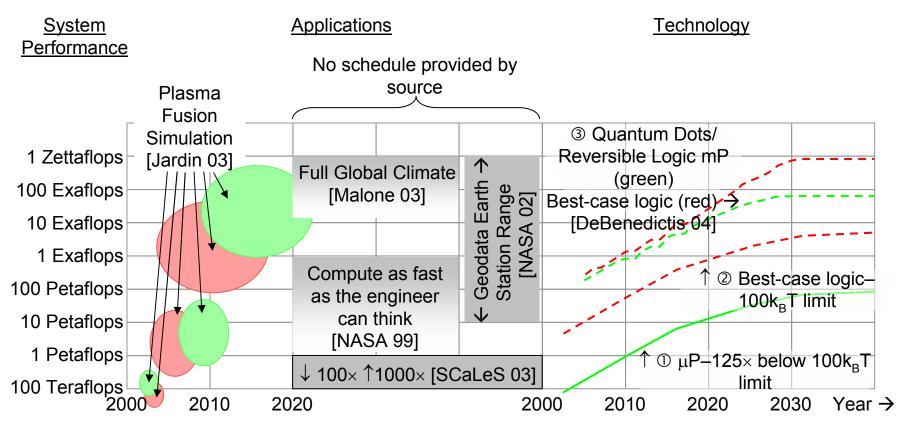
Erik P. DeBenedictis

Sandia National Laboratories





### **Applications and Computer Technology**



[Jardin 03] S.C. Jardin, "Plasma Science Contribution to the SCaLeS Report," Princeton Plasma Physics Laboratory, PPPL-3879 UC-70, available on Internet.
[Malone 03] Robert C. Malone, John B. Drake, Philip W. Jones, Douglas A. Rotman, "High-End Computing in Climate Modeling," contribution to SCaLeS report.
[NASA 99] R. T. Biedron, P. Mehrotra, M. L. Nelson, F. S. Preston, J. J. Rehder, J. L. Rogers, D. H. Rudy, J. Sobieski, and O. O. Storaasli, "Compute as Fast as the Engineers Can Think!"
NASA/TM-1999-209715, available on Internet.

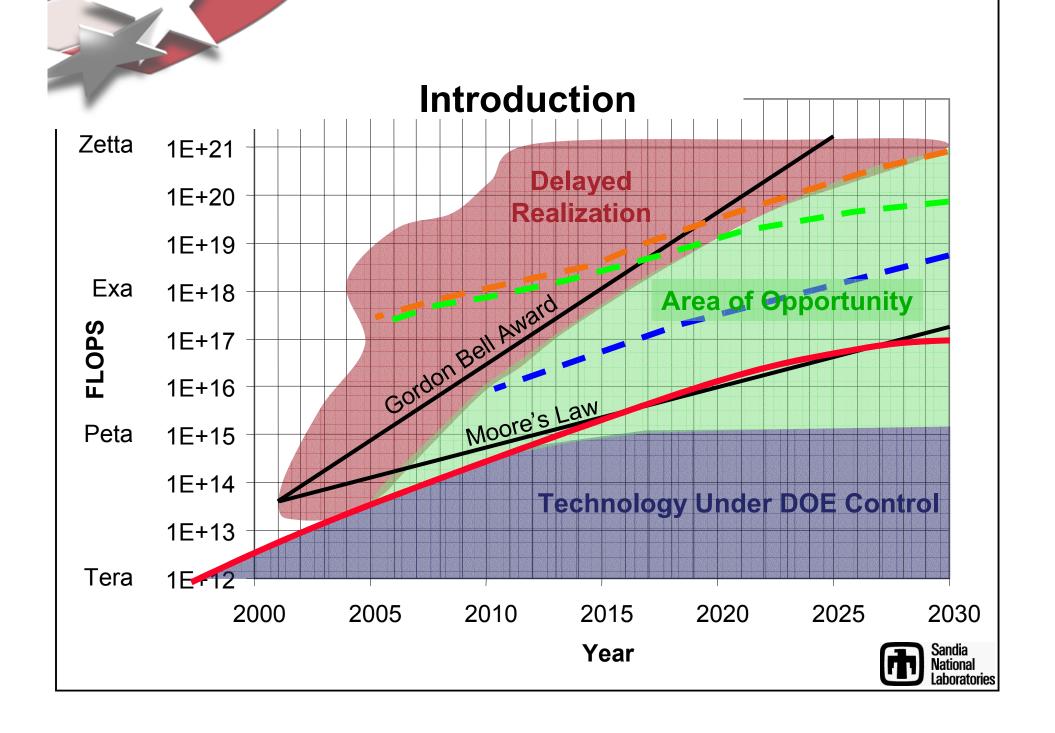
s**Sandia** 

**National** 

Laboratories

[NASA 02] NASA Goddard Space Flight Center, "Advanced Weather Prediction Technologies: NASA's Contribution to the Operational Agencies," available on Internet. [SCaLeS 03] Workshop on the Science Case for Large-scale Simulation, June 24-25, proceedings on Internet a http://www.pnl.gov/scales/.

[DeBenedictis 04], Erik P. DeBenedictis, "Matching Supercomputing to Progress in Science," July 2004. Presentation at Lawrence Berkeley National Laboratory, also pushed a National Laboratories SAND report SAND2004-3333P. Sandia technical reports are available by going to http://www.sandia.gov and accessing the technical library.





### **Outline**

- Applications of the Future
- Limits of Moore's Law
- An Expert System/Optimizer for Supercomputing
- Reaching to Zettaflops
- Roadmap and Future Directions





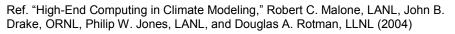
#### **Global Climate**

- Objective
  - Collect data about Earth
  - Model climate into the future
  - Provide "decision support" and ability to "mitigate"
- Approaches
  - Climate models exist, but need they more resolution, better physics, and better initial conditions (observations of the Earth)
- Computer Resources Required
  - Increments over current workstation on next slide



### **FLOPS Increases for Global Climate**

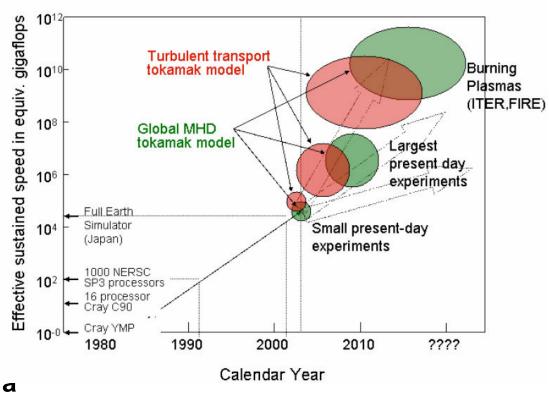
	Issue	Scaling
1 Zettaflops	Ensembles, scenarios 10×	Embarrassingly Parallel
100 Exaflops	Run length 100×	Longer Running Time
1 Exaflops ←	New parameterizations 100×	More Complex Physics
10 Petaflops	Model Completeness 100×	More Complex Physics
100 Teraflops	Spatial Resolution 10 <sup>4</sup> × (10 <sup>3</sup> ×-10 <sup>5</sup> ×)	Resolution
10 Gigaflops ←	Current	





### Requirements for Plasma Simulation

- Very high peak perform ance requirements
  - but seeking algorithmic improvements
- Two methods
  - Red regions very scalable, Monte Carl
  - Green regions N<sup>4</sup> scaling (FEM)
- Long term objective
  - Merge methods into a single code



Ref. "Plasma Science Contribution to the SCaLeS Report," S.C. Jardin, October 2003





#### **NASA Climate Earth Station**

Based on these inputs, various portions of the Modeling and Data Assimilation System will require anywhere from 10<sup>7</sup> to 10<sup>13</sup> GFLOPS of computational resources. In other words, the range of computational resources needed is 10<sup>16</sup> to 10<sup>21</sup> Floating Point Operations per Second. For the curious, the range can also be stated as 10 PetaFLOPS to 1 ZettaFLOPS.

#### 4.1.2. Anticipated Computing Technology Capabilities

At first glance, the numbers discussed in the previous section appear so high as to be impossibly ludicrous. However, with the expected growth in computing capabilities, the lower end of this spectrum actually falls within the domain of possibility.

"Advanced Weather Prediction Technologies:
 NASA's Contribution to the Operational Agencies,"
 Gap Analysis Appendix, May 31, 2002





#### **NASA Work Station**

- "...the ultimate goal of making the computing underlying the design process so capable that it no longer acts as a brake on the flow of the creative human thought..."
- Requirement 3 Exaflops
- Note: In the context of this report, this requirement is for one or a few engineers, not a supercomputer center!

NASA/TM-1999-209715



Compute as Fast as the Engineers Can Think!

ULTRAFAST COMPUTING TEAM FINAL REPORT

R. T. Biedron, P. Mehrotra, M. L. Nelson, F. S. Preston, J. J. Rehder, J. L. Rogers, D. H. Rudy, J. Sobieski, and O. O. Storaasli Langley Research Center, Hampton, Virginia





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### \*\*\* This is a Preview \*\*\*

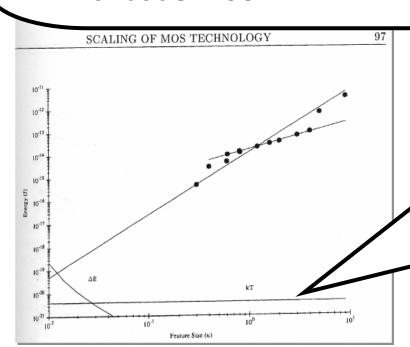
	Best-Case Logic	Microprocessor Architecture	•	Physical Factor	Source of Authority
	1.5 Yottaops			Landauer limit 600KW/(100k <sub>B</sub> T)	Esteemed physicists
				Derate 20,000 convert logic ops to floating point	Floating point engineering (64 bit precision)
Expert Opinion	100 Exaflops ← 125	800 Petaflops :1 →		Derate for manufacturing margin (4×)	Estimate
Estimate	25 Exaflops	200 Petaflops		Uncertainty (6×)	Gap in chart
	4 Exaflops	32 Petaflops		Improved devices (4×)	Estimate
	1 Exaflops	8 Petaflops		Projected ITRS improvement to 22 nm	ITRS committee of experts
•	: Supercomputer	00 Tarreflana		(100×)	
is size & cost of Red Storm: \$100M budget; consumes		80 Teraflops		Lower supply voltage (2×)	ITRS committee of experts
1.8 MW wal to active co	ll power; 600 KW mponents	40 Teraflops	<b>←</b>	Red Storm	contract
			L		National Laborato



#### **Thermal Noise Limit**

This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function.

R. Landauer 1961



Irreversability and Heat Generation in the Computing Process

As a comparison of the Computing Process

As a computing Process

As a comparison of the Compu

kT "helper line," drawn out of the reader's focus because it wasn't important at the time of writing

Carver Mead, Scaling of MOS Technology, 1994



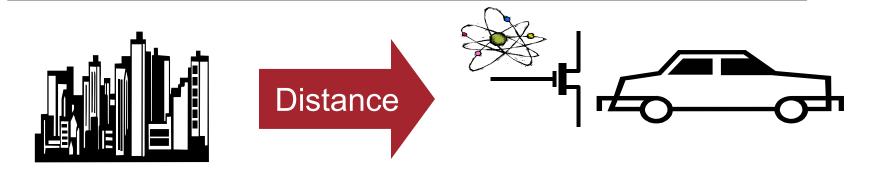
### **Metaphor: FM Radio on Trip to Seattle**

- You drive to Seattle listening to FM radio
- Music clear for a while, but noise creeps in and then overtakes music
- Analogy: You live out the next dozen years buying PCs every couple years
- PCs keep getting faster
  - clock rate increases
  - fan gets bigger
  - won't go on forever
- Why...see next slide

Details: Erik DeBenedictis, "Taking ASCI Supercomputing to the End Game," SAND2004-0959



### FM Radio and End of Moore's Law



Driving away from FM transmitter→less signal Noise from electrons → no change



Increasing numbers of gates → less signal power Noise from electrons → no change



### **Amount of Reliability Needed**

- We expect computers to be reliable
- A future supercomputer will perform 10<sup>30</sup>-10<sup>40</sup> operations in its lifetime
- Error rate should be < 10<sup>-30</sup>
   10<sup>-40</sup>
- Reliability due to thermal noise about e<sup>-E/kt</sup>
- Need about e<sup>-100</sup> error rate, or 100 k<sub>B</sub>T switching energy

SNR (db)	Power Ratio	P <sub>error</sub>
10	10	3.9×10 <sup>-6</sup>
14	25	6.8×10 <sup>-13</sup>
18	63	1.4×10 <sup>-29</sup>
22	160 Noise Lim	3.3×10 <sup>-71</sup>
26	400	1.8×10 <sup>-175</sup>
30	1,000 2016	4.5×10 <sup>-437</sup>
34	2,500	7.1×10 <sup>-1094</sup>
38	6,300	2.2×10 <sup>-2743</sup>
42	16,000	1.8×10 <sup>-6886</sup>
46	40,000	3.8×10 <sup>-17293</sup>
50	100,000 Today	3.2×10 <sup>-43433</sup>
54	250,000	8.1×10 <sup>-10194</sup>
58	630,000	1.8×10 <sup>-274025</sup>
62	1,500,000	9.6×10 <sup>-688315</sup>

$$q := \int_{t}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} dx; t \rightarrow \sqrt{2 * 10^{\frac{5nx}{10}}}$$





#### **Noise Levels**

- 0 db Limit of hearing
- 20 db Rustling leaves
- 40-50 db Typical neighborhood
- 60-70 db Normal conversation
- 80 db Telephone dial tone
- 85 db City traffic inside car
- 90 db Train whistle @500'
- 95 db Subway train @200'
- 90-95 db Ear damage

- Today: 50 db
  - Thermal noise:Logic::Rustling leaves:Talking
- 2016: 30 db
  - Thermal noise:Logic:: Talking:Train Whistle
- Reliability limit 20 db
  - Thermal noise:Logic::Outsideneighborhood:Talking



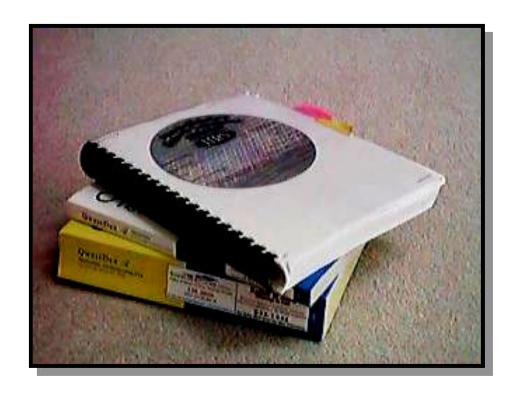
#### **Personal Observational Evidence**

- Have radios become better able to receive distant stations over the last few decades with a rate of improvement similar to Moore's Law?
- You judge from your experience, but the answer should be that they have not.
- Therefore, electrical noise does not scale with Moore's Law.





- Generalization of Moore's Law
  - Projects many parameters
  - Years through 2016
  - Includes justification
  - Panel of experts
    - known to be wrong
  - Size between
     Albuquerque white and yellow pages





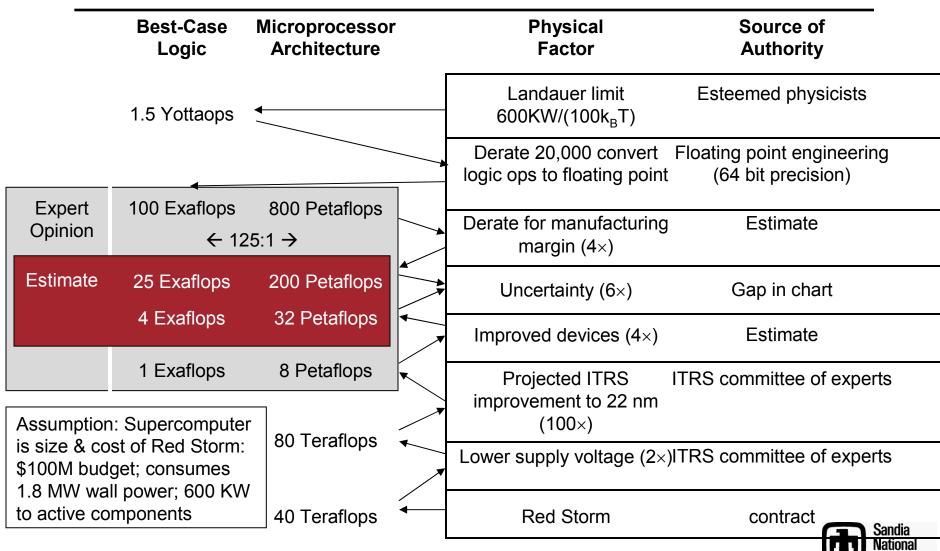
## **Semiconductor Roadmap**

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ PITCH (nm)	45	32	22
MPU / ASIC ½ PITCH (nm)		35	25
MPU PRINTED GATE LENGTH (nm)	25	18	13
MPU PHYSICAL GATE LENGTH (nm)	18	13	9
Physical gate length high-performance (HP) (nm) [1]	18	13	9
Equivalent physical oxide thickness for high-performance $T_{ox}$ (EOT)( nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.5	0.5	0.5
$T_{ox}$ electrical equivalent (nm) [4]	1.2	1.0	0.9
Nominal power supply voltage $(V_{dd})$ $(V)$ [5]	0.6	0.5	0.4
Nominal high-performance NMOS sub threshold leakage current, $I_{sd,leak}$ (at 25 ° C) ( $\mu$ A/ $\mu$ m) [6]	3	7	10
Nominal high-performance NMOS saturation drive current , $I_{dd}$ (at $V_{dd}$ at 25 ° C) ( $\mu A/\mu m$ ) [7]	1200	1500	1500
Required percent current-drive "mobility/transconductance improvement" [8]	30%	70%	100%
Parasitic source/drain resistance (Rsd) (ohm to be 100	110	90	80
	25%	30%	35%
Parasitic source/drain resistance (Rsd) pe Parasitic capacitance percent of ideal gat 1,000 k <sub>B</sub> T/transistor	31%	36%	42%
High-performance NMOS device $\tau$ (C <sub>gate</sub> * $V_{dd}/I_{dd}$ -NMOS)(ps) [12]	0.39	0.22	0.15
Relative device performance [13]		7.2	10.7
Energy per (W/L <sub>gate</sub> =3) device switching transition ( $C_{gate}*(3*L_{gate})*V^2$ ) (fJ/Device) [14]	0.015	0.007	0.002
Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	9.7E-08	1.4E-07	1.1E-07

White—Manufacturable Solutions Exist, and Are Being Optimized Yellow—Manufacturable Solutions are Known Red—Manufacturable Solutions are NOT Known



### **Leadership Class Supercomputer Limits**





### **Outline**

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### **Expert System for Future Supercomputers**

- Applications Modeling
  - Runtime  $T_{run} = f_1(n, design)$
- Technology Roadmap
  - Gate speed =  $f_2$ (year),
  - chip density =  $f_3$ (year),
  - $-\cos t = (n, design), ...$
- Scaling Objective Function
  - I have \$C<sub>1</sub> & can wait T<sub>run</sub>=C<sub>2</sub> seconds. What is the biggest n I can solve in year Y?

 Use "Expert System" To Calculate:

Max n:  $\$< C_1$ ,  $T_{run} < C_2$ All designs

Report:

**Floating operations** 

T<sub>run</sub>(n, design)

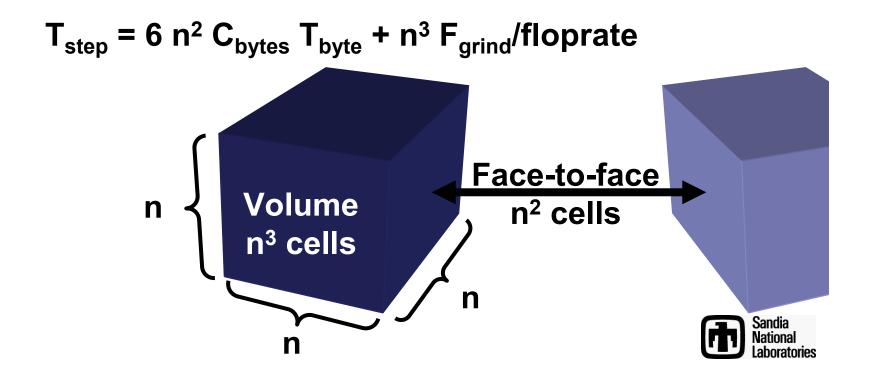
and illustrate "design"



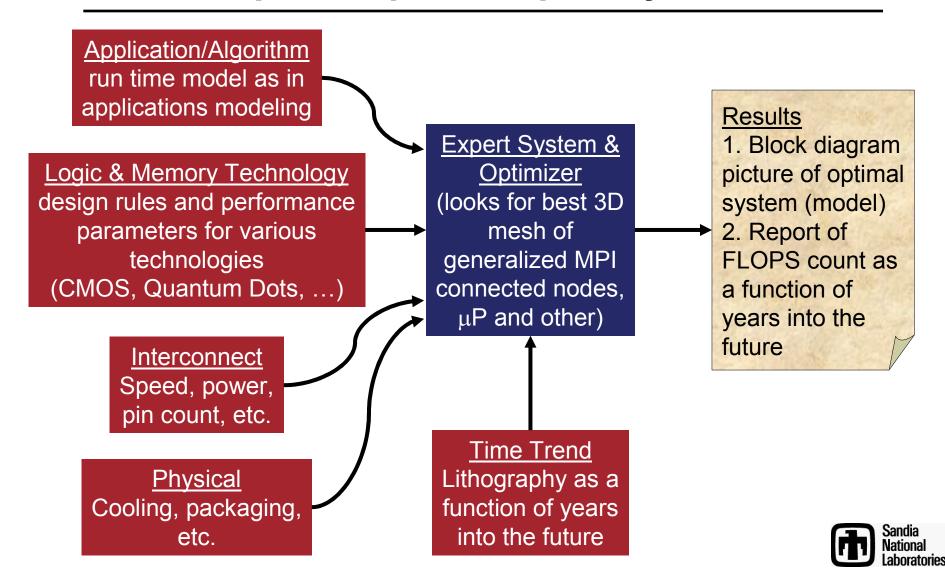
### **Analytical Runtime Model**

- Simple case: finite difference equation
- Each node holds n×n×n grid points

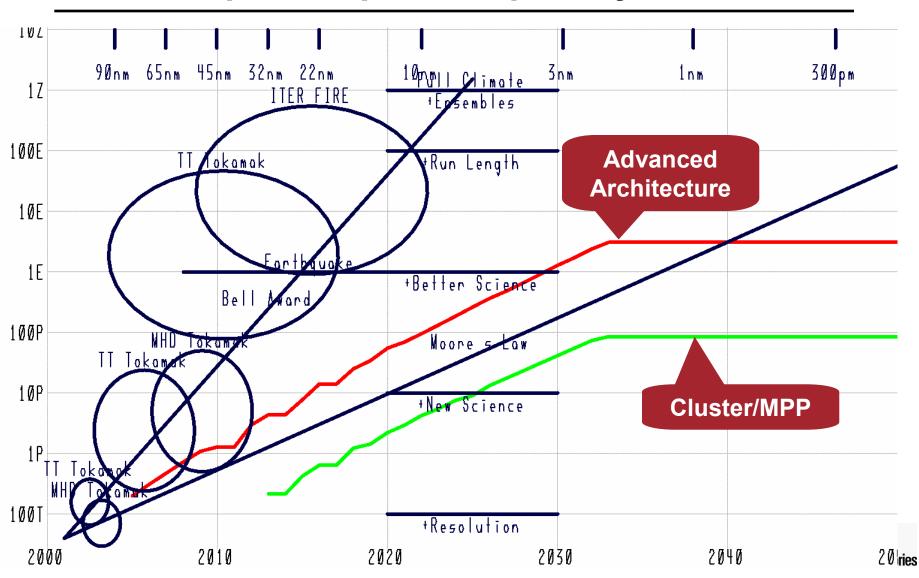
- Volume-area rule
  - Computing  $\infty$  n<sup>3</sup>
  - Communications  $\infty$  n<sup>2</sup>



### Supercomputer Expert System



### **Supercomputer Expert System**

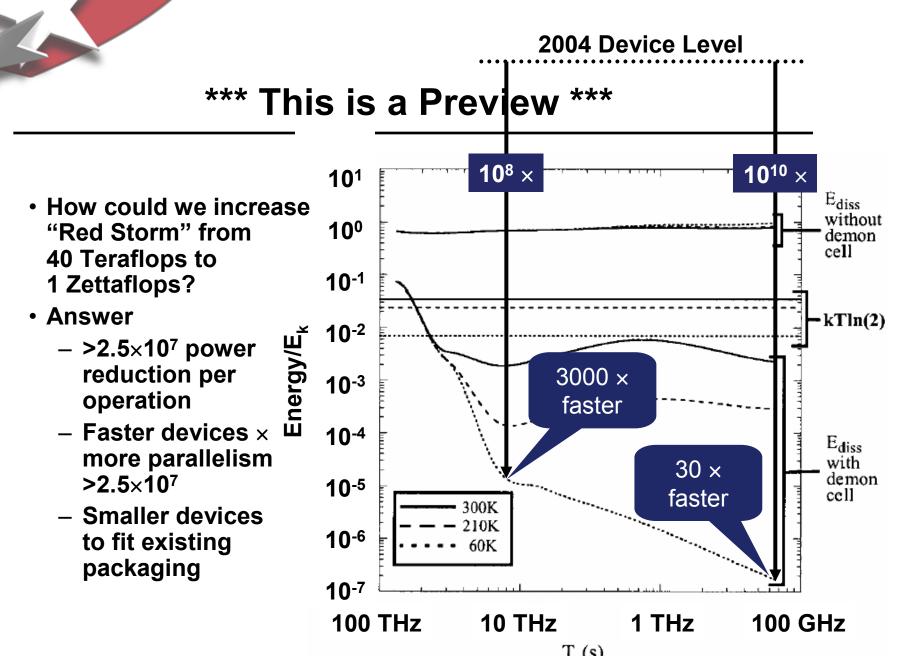




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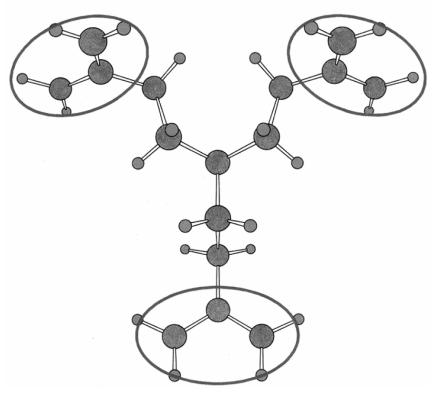


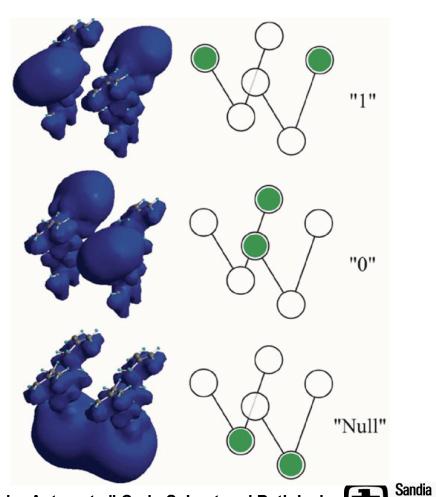


Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent JOURNAL OF APPLIED PHYSICS 15 JULY 2003

## **An Exemplary Device: Quantum Dots**

 Pairs of molecules create a memory cell or a logic gate



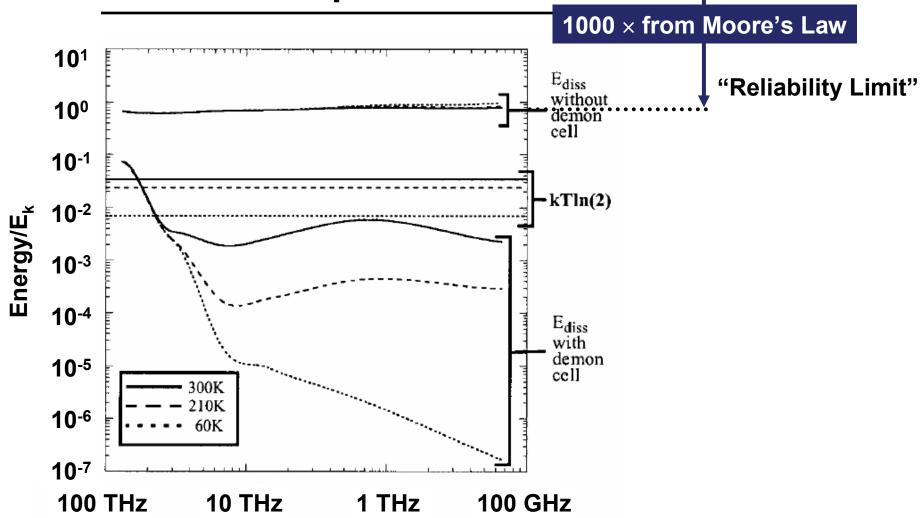


**National** 

Ref. "Clocked Molecular Quantum-Dot Cellular Automata," Craig S. Lent and Beth Isakse IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003



Step 1: Moore's law



 $T_{\rm c}(s)$  Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent, JOURNAL OF APPLIED PHYSICS 15 JULY 2003

Sandia National Laboratories

2004 Device Level **Step 2: Energy Recycling** 1000 × 10<sup>1</sup> Ediss "Reliability Limit" without **10**<sup>0</sup> demon cell 150 × from "recycling" **10**<sup>-1</sup> "Landauer Limit" -kTln(2) 10<sup>-2</sup> Energy/E<sub>k</sub> **10**-3 10-4  $E_{\text{diss}} \\$ with demon **10**-5 cell 300K 210K **10**-6 10-7

1 THz

100 THz

10 THz

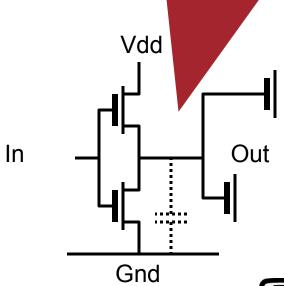


100 GHz

### Today's Universal Logic & Reliability Limit

- Today's logic operates on a simple principle
  - Create a "1" by taking charge from the positive supply
  - Create a "0" by sending charge to the negative supply
- Energy Consumption
  - Each gate switch generates  $E_{sw} = \frac{1}{2} \text{ CV}^2 > \frac{100 \text{ k}_B \text{T}}{2}$

Signal energy must be greater than ~100 k<sub>B</sub>T to avoid spontaneous glitches. To change a bit, convert energy to heat.



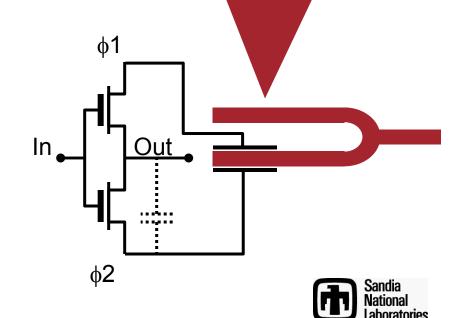




### "Recycling" Power

- The 100k<sub>B</sub>T limit appears unbeatable, but the energy can be "recycled"
- Diagram shows a "SCRL" circuit with regular transistors
- Power comes through a largely loss less resonant device (tuning fork)
- No apology offered for the mechanical device; this is the price of progress

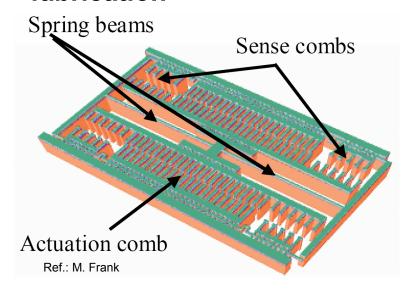
Signal energy must be greater than ~100 k<sub>B</sub>T to avoid spontaneous glitches. However, signal energy is recycled by tuning fork



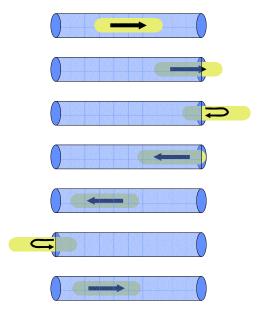


#### **Resonant Clocks**

- Tuning Fork
  - Nice idea but slow
- MEMs Resonator
  - Moderate speed and compatible with silicon fabrication



- Carbon Nanotube
  - Simulated to 50 GHz but not known how to fabricate at present

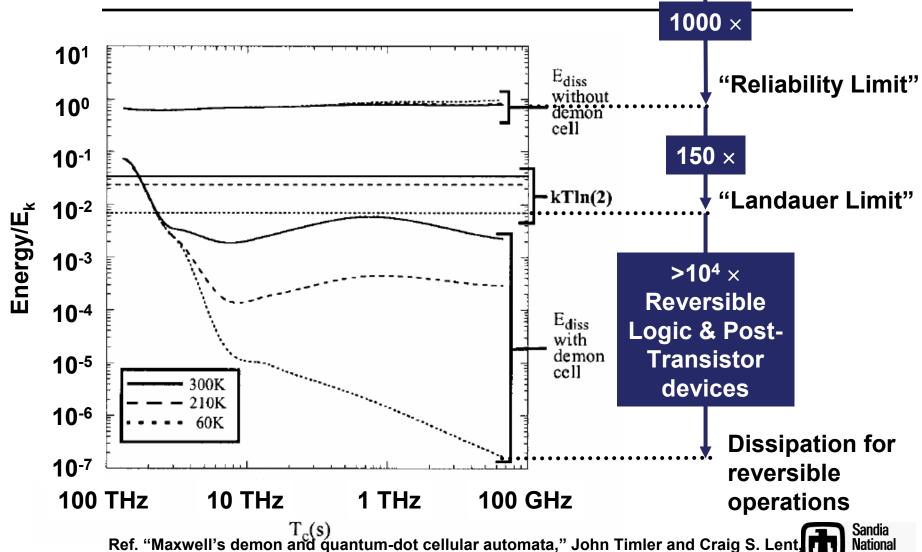




2004 Device Level

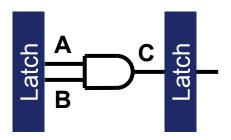
Laboratories

## Step 3: Reversibility & New Devices



 $T_{c}(s)$  Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent, **JOURNAL OF APPLIED PHYSICS 15 JULY 2003** 

# **How Much Heat to Discharge a Capacitor?**

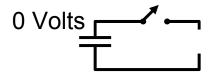


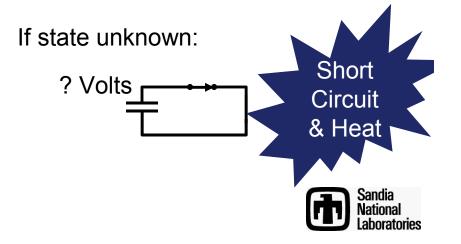
- At some point it will be necessary for signals A and B to change to some new values
- We can avoid generating heat if we know the previous value

If charged:



If discharged:

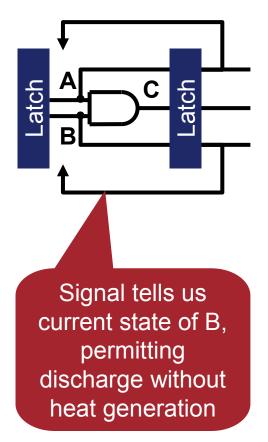






### **Reversible Gates**

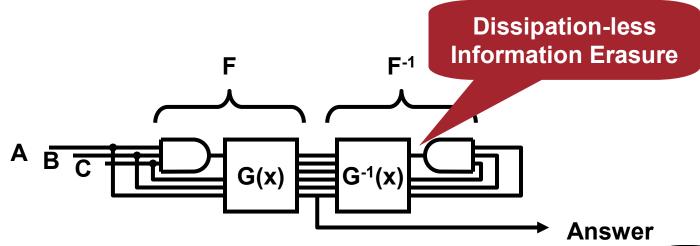
- If we save the state of every signal, we can discharge the capacitors associated with signals without heat
- There are also gates where the state is not saved but can be reconstructed
  - Fredkin, Toffoli, CNOT
- However, this causes an increase in the number of signals







- Any function can be made reversible by saving its inputs, but this increases the number of signals
- Diagram below outlines an asymptotically zeroenergy way to perform the AND function, in composition with other logical operations





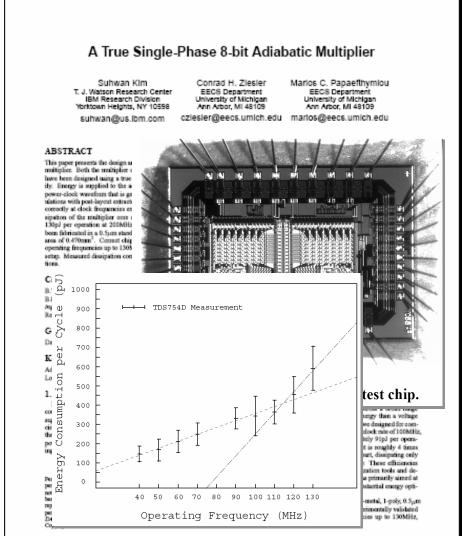
# Two Key Points About Reversible Logic

- You saw a chart showing 10<sup>5</sup>-10<sup>7</sup> improvement in power performance due to reversibility
- Reversible logic design principles are different from today's logic
  - It will be unfamiliar to today's engineers
  - Many design tools will require rewriting





- 8×8 Multiplier Designed, Fabricated, and Tested by IBM & University of Michigan
- Power savings was up to 4:1





# **CPU Design**

- Leading Thoughts
  - Implement CPU logic using reversible logic
    - High efficiency for the component doing the most logic
  - Implement state and memory using conventional logic
    - Low efficiency, but not many operations
  - Permits programming much like today

Reversible Logic

Irreversible Logic

**CPU Logic CPU State** Conventional Memory

## **Reversible Microprocessor Status**

### Status

- Subject of Ph. D. thesis
- Chip laid out (no floating point)
- RISC instruction set
- C-like language
- Compiler
- Demonstrated on a PDE
- However: really weird and not general to program with +=, -=, etc. rather than =

### Reversible Computer Engineering and Architecture

Carlin Vieri
MIT Artificial Intelligence Laboratory

Tom Knight: Committee chairman Gerald Sussman, Gill Pratt: readers

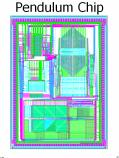
### Pendulum Reversible Processor

- # 200,000 Transistors
- # 18 Instructions
- 3 → SCRL
- **#** 50 mm<sup>2</sup> in HP14
- **#** 180 Pins

△32 power supplies

# 2 Person years for schematics and layout

PhD Thesis Defe





## **Upside Potential of Quantum Dots**

### THE RESERVE OF THE PARTY OF

### Manwell's demon and quantum-dot cellular automata

Arts Tories and Couly &  $\tan^{2}\theta$  . By several of the class, then then, below 0.01(Contract Ferrage 1990), was great in April 1990).

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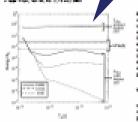
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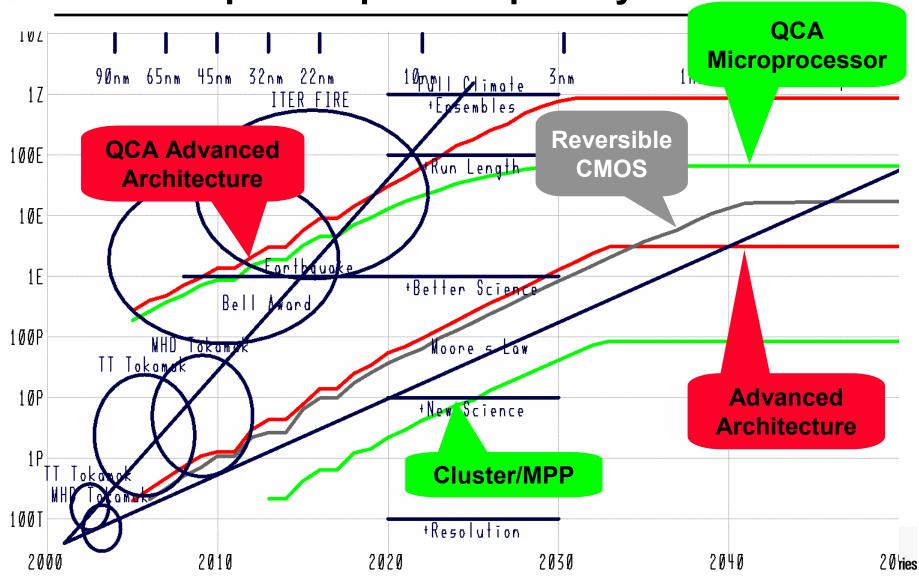
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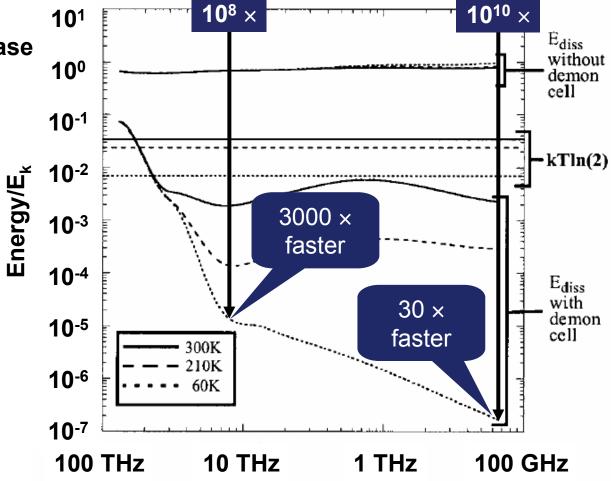


# 1 Zettaflops Leadership Supercomputer

How could we increase "Red Storm" from 40 Teraflops to 1 Zettaflops?

### Answer

- >2.5×10<sup>7</sup> power reduction per operation
- Smaller devices to fit existing packaging
- Faster devices × more parallelism
   >2.5×10<sup>7</sup>



2004 Device Level

Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent JOURNAL OF APPLIED PHYSICS 15 JULY 2003



### **Outline**

- Applications of the Future
- Limits of Moore's Law
- An Expert System/Optimizer for Supercomputing
- Reaching to Zettaflops
- Roadmap and Future Directions





### **Conclusions**

- A review of key problems in science that can be solved with supercomputers reveals a continuum of FLOPS "demand" up to 1 Zettaflops
- A review of "the physics of computation" reveals a progression of technologies offering a progressively larger "supply" of FLOPS for up to at least 1 Zettaflops
- Supply and demand are thus about the same

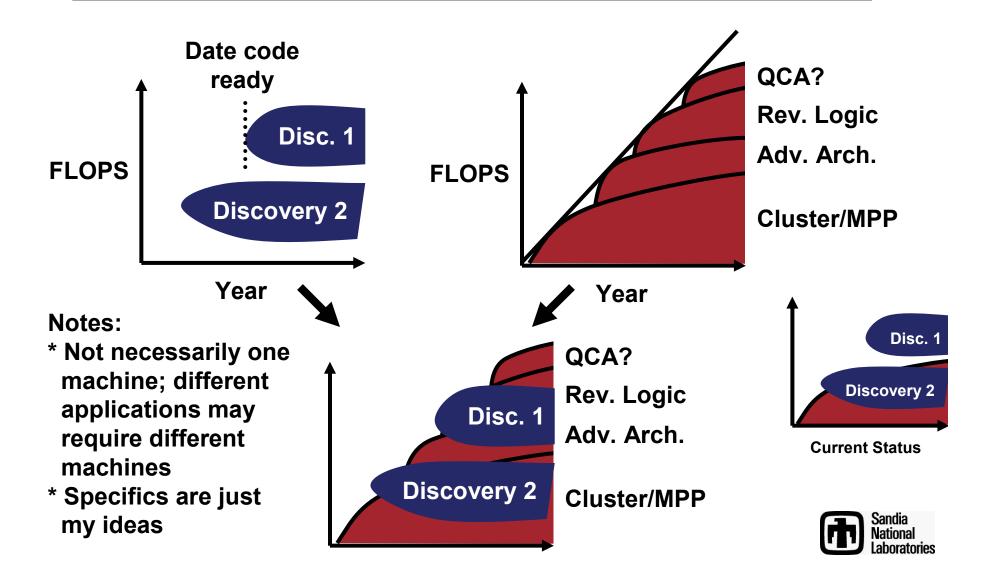




- Don't believe me? Believe the Experts
- Workshop Agenda October
  - Applications session Climate expert Phil Jones
  - Advanced Architectures PIM expert Peter Kogge
  - Limits of Current Architectures Me
  - Limits Panel I: Limits of Current Technology
  - New Logic Reversible Logic Expert Michael Frank
  - New Devices Quantum Dot Developer Craig Lent
  - Limits Panel II: Opportunities with Innovation



## Where To Go Next II: Roadmap



## Where to Go Next III: PNNL Can Help

- What is the largest FLOPS rate that can be justified on the basis of scientific discovery for PNNL applications?
  - Not exactly for today's applications, but for scaled up problems of the same type
  - If your answer is
    - < 1 Zettaflops: you will be in good company</li>
    - > 1 Zettaflops, you can be the high performance leader!
- This information would be helpful in justifying increasingly powerful supercomputers and planning scientific discoveries

