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Reversible Logic for Supercomputing

Presented at RC'05:
The First Int'l. Workshop on Reversible Computing

Erik P. DeBenedictis
Sandia National Laboratories

May 5, 2005

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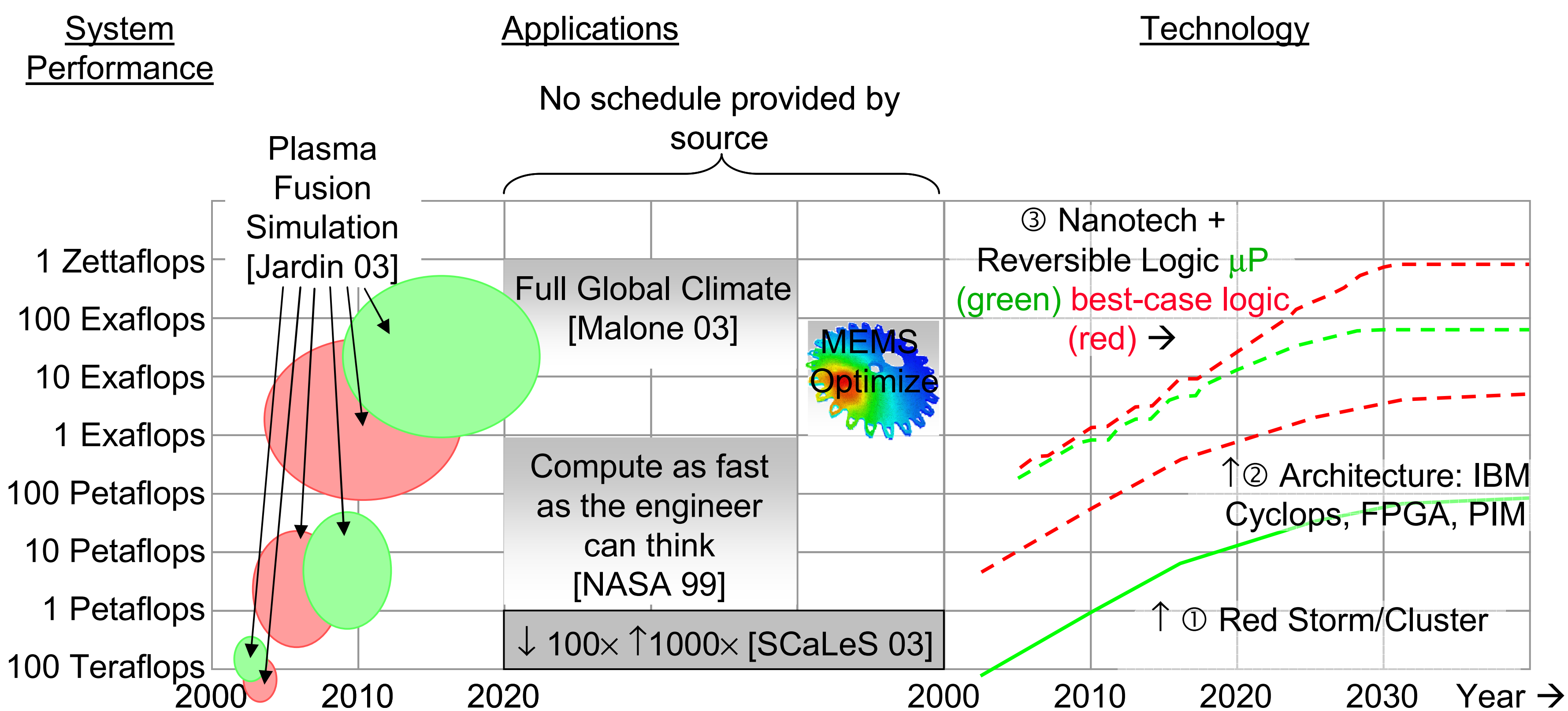
Applications and $100M Supercomputers



[Jardin 03] S.C. Jardin, "Plasma Science Contribution to the SCaLeS Report," Princeton Plasma Physics Laboratory, PPPL-3879 UC-70, available on Internet.
[Malone 03] Robert C. Malone, John B. Drake, Philip W. Jones, Douglas A. Rotman, "High-End Computing in Climate Modeling," contribution to SCaLeS report.
[NASA 99] R. T. Biedron, P. Mehrotra, M. L. Nelson, F. S. Preston, J. J. Rehder, J. L. Rogers, D. H. Rudy, J. Sobieski, and O. O. Storaasli, "Compute as Fast as the Engineers Can Think!" NASA/TM-1999-209715, available on Internet.
[SCaLeS 03] Workshop on the Science Case for Large-scale Simulation, June 24-25, proceedings on Internet a http://www.pnl.gov/scales/.
[DeBenedictis 04], Erik P. DeBenedictis, "Matching Supercomputing to Progress in Science," July 2004. Presentation at Lawrence Berkeley National Laboratory, also published as Sandia National Laboratories SAND report SAND2004-3333P. Sandia technical reports are available by going to http://www.sandia.gov and accessing the technical library.

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Objectives and Challenges

- Could reversible computing have a role in solving important problems?
  - Maybe, because power is a limiting factor for computers and reversible logic cuts power
- However, a complete computer system is more than “low power”
  - Processing, memory, communication in right balance for application
  - Speed must match user’s impatience
  - Must use a real device, not just an abstract reversible device

Outline

- An Exemplary Zettaflops Problem
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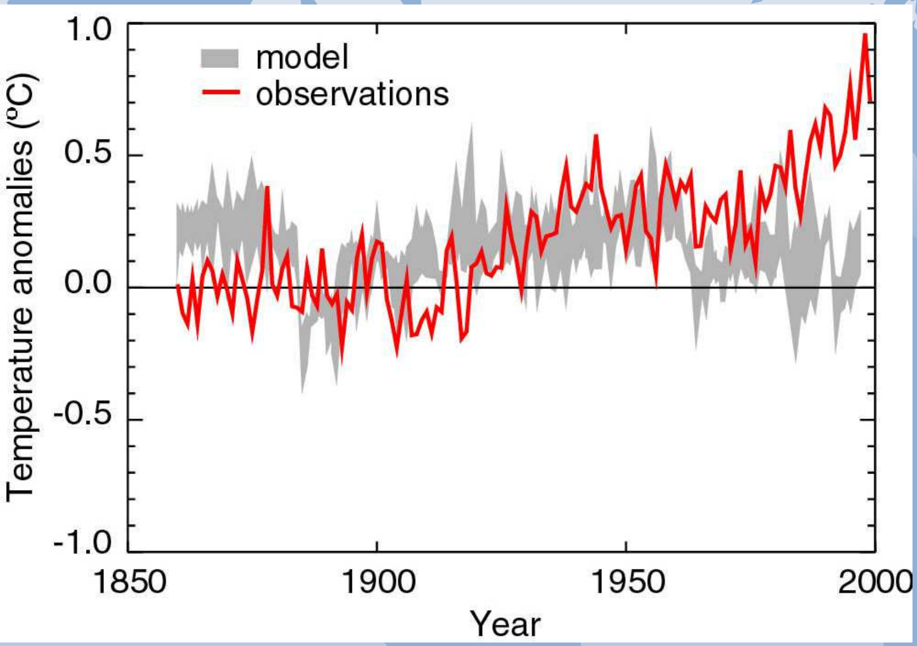
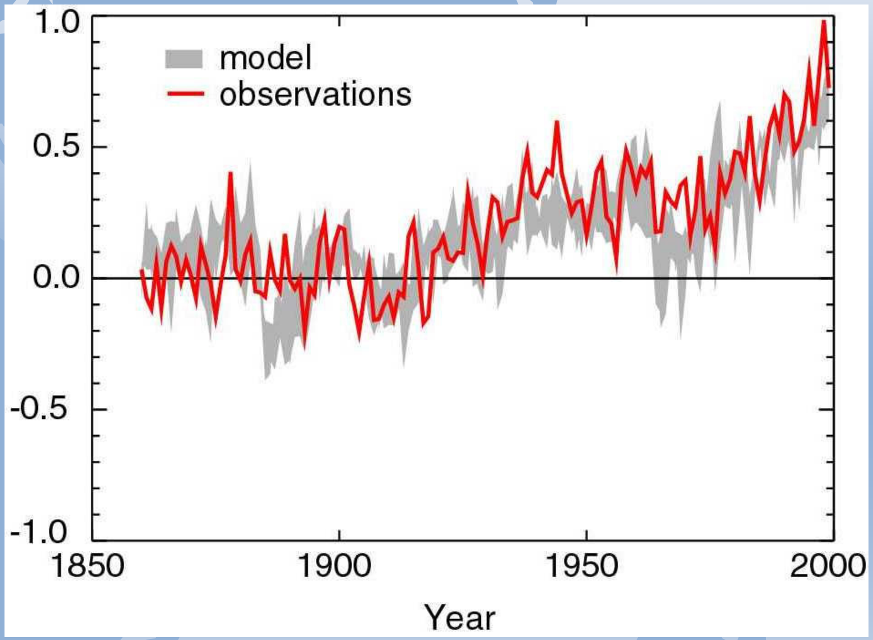
Simulation of Global Climate





Stott et al, Science 2000

“Simulations of the response to natural forcings alone … do not explain the warming in the second half of the century”

“..model estimates that take into account both greenhouse gases and sulphate aerosols are consistent with observations over this*period” - IPCC 2001

FLOPS Increases for Global Climate

1 Zettaflops

100 Exaflops

1 Exaflops

10 Petaflops

100 Teraflops

10 Gigaflops

Issue	Scaling
Ensembles, scenarios $10\times$	Embarrassingly Parallel
Run length $100\times$	Longer Running Time
New parameterizations $100\times$	More Complex Physics
Model Completeness $100\times$	More Complex Physics
Spatial Resolution $10^4\times$ ($10^3\times$-$10^5\times$)	Resolution
Clusters Now In Use (100 nodes, 5% efficient)	

Ref. "High-End Computing in Climate Modeling," Robert C. Malone, LANL, John B. Drake, ORNL, Philip W. Jones, LANL, and Douglas A. Rotman, LLNL (2004)

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*** This is a Preview ***

Best-Case Logic	Microprocessor Architecture
2×10^{24} logic ops/s	
100 Exaflops	800 Petaflops
← 125:1 →	
25 Exaflops	200 Petaflops
4 Exaflops	32 Petaflops
1 Exaflops	8 Petaflops
	80 Teraflops
	40 Teraflops

Expert Opinion

Estimate

Assumption: Supercomputer is size & cost of Red Storm: US$100M budget; consumes 2 MW wall power; 750 KW to active components

Physical Factor	Source of Authority
Reliability limit 750KW/(80k_BT)	Esteemed physicists (T=60°C junction temperature)
Derate 20,000 convert logic ops to floating point	Floating point engineering (64 bit precision)
Derate for manufacturing margin (4×)	Estimate
Uncertainty (6×)	Gap in chart
Improved devices (4×)	Estimate
Projected ITRS improvement to 22 nm (100×)	ITRS committee of experts
Lower supply voltage (2×)	ITRS committee of experts
Red Storm	contract

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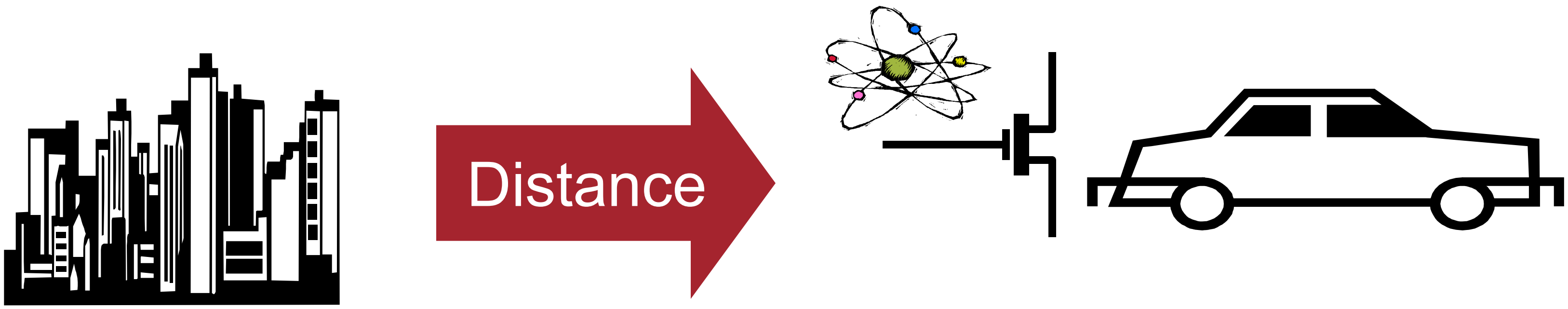
Metaphor: FM Radio on Trip to in USA

- You drive to a distant listening to FM radio
- Music clear for a while, but noise creeps in and then overtakes music

- Analogy: You live out the next dozen years buying PCs every couple years
- PCs keep getting faster
  – clock rate increases
  – fan gets bigger
  – won't go on forever
- Why…see next slide

Details: Erik DeBenedictis, "Taking ASCI Supercomputing to the End Game," SAND2004-0959

FM Radio and End of Moore's Law



Driving away from FM transmitter→less signal
Noise from electrons → no change

Increasing numbers of gates→less signal power
Noise from electrons → no change

Scientific Supercomputer Limits

Best-Case Logic	Microprocessor Architecture
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Supercomputer Expert System

Application/Algorithm
run time model as in applications modeling

Logic & Memory Technology
design rules and performance parameters for various technologies (CMOS, Quantum Dots, C Nano-tubes …)

Interconnect
Speed, power, pin count, etc.

Physical
Cooling, packaging, etc.

Expert System & Optimizer
(looks for best 3D mesh of generalized MPI connected nodes, µP and other)

Time Trend
Lithography as a function of years into the future

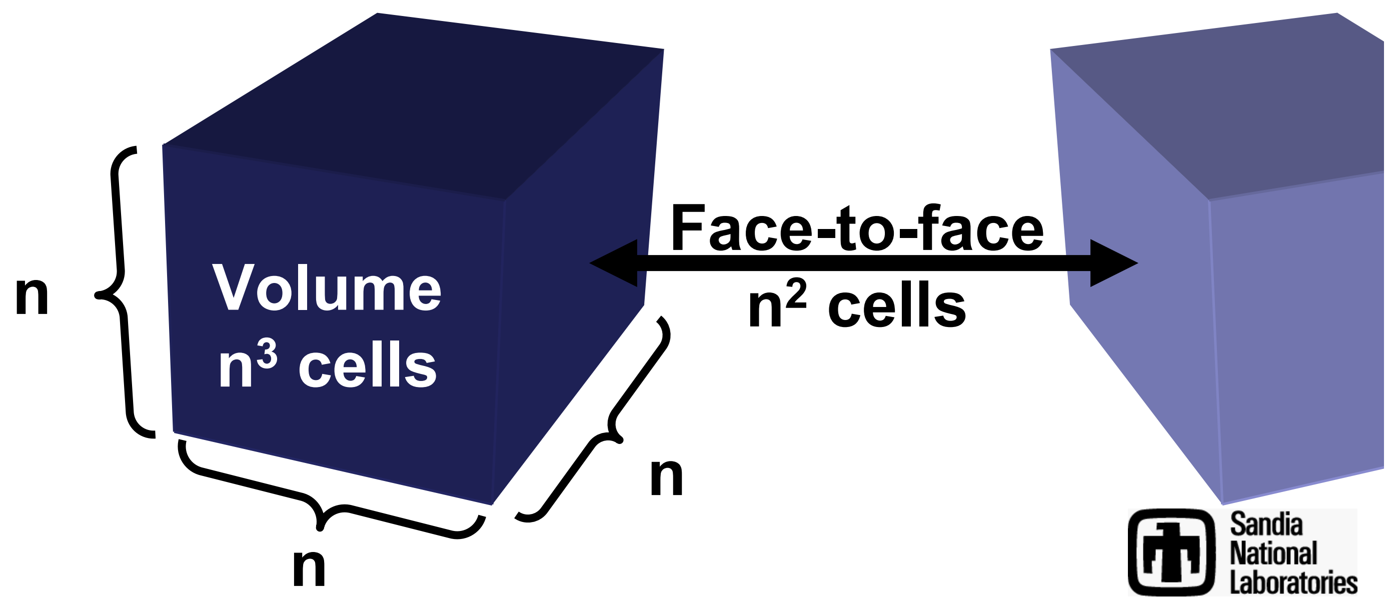
Results
1. Block diagram picture of optimal system (model)
2. Report of FLOPS count as a function of years into the future

Sample Analytical Runtime Model

- Simple case: finite difference equation
- Each node holds n×n×n grid points

- Volume-area rule
  - Computing $\propto n^3$
  - Communications $\propto n^2$

$$T_{step} = 6\, n^2\, C_{bytes}\, T_{byte} + n^3\, F_{grind}/\text{floprate}$$



Expert System for Future Supercomputers

- Applications Modeling
  - Runtime
    $T_{run} = f_1(n, \text{design})$
- Technology Roadmap
  - Gate speed = $f_2(\text{year})$,
  - chip density = $f_3(\text{year})$,
  - cost = $\$(n, \text{design})$, …
- Scaling Objective Function
  - I have $\$C_1$ & can wait $T_{run}=C_2$ seconds. What is the biggest n I can solve in year Y?

- Use "Expert System" To Calculate:

$$\max_{\text{All designs}} \quad n: \$<C_1,\ T_{run}<C_2$$

- Report:

$$\frac{\text{Floating operations}}{T_{run}(n, \text{design})}$$

and illustrate "design"

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The Big Issue

- **Initially, didn't meet constraints**

More Parallelism

Scaled Climate Model

2D → 3D mesh,
one cell per processor

Parallelize cloud-resolving model and ensembles

One Barely Plausible Solution

Consider special purpose logic with fast logic and low-power memory

Consider only highest performance published nanotech device QDCA

Initial reversible nanotech

More Device Speed

ITRS Device Review 2016 + QDCA

Technology	Speed (min-max)	Dimension (min-max)	Energy per gate-op	Comparison
CMOS	30 ps-1 μs	8 nm-5 μm	4 aJ	
RSFQ	1 ps-50 ps	300 nm- 1μm	2 aJ	Larger
Molecular	10 ns-1 ms	1 nm- 5 nm	10 zJ	Slower
Plastic	100 μs-1 ms	100 μm-1 mm	4 aJ	Larger+Slower
Optical	100 as-1 ps	200 nm-2 μm	1 pJ	Larger+Hotter
NEMS	100 ns-1 ms	10-100 nm	1 zJ	Slower+Larger
Biological	100 fs-100 μs	6-50 μm	.3 yJ	Slower+Larger
Quantum	100 as-1 fs	10-100 nm	1 zJ	Larger
QDCA	100 fs-10ps	1-10 nm	1 yJ	Smaller, faster, cooler

Data from ITRS ERD Section, data from Notre Dame

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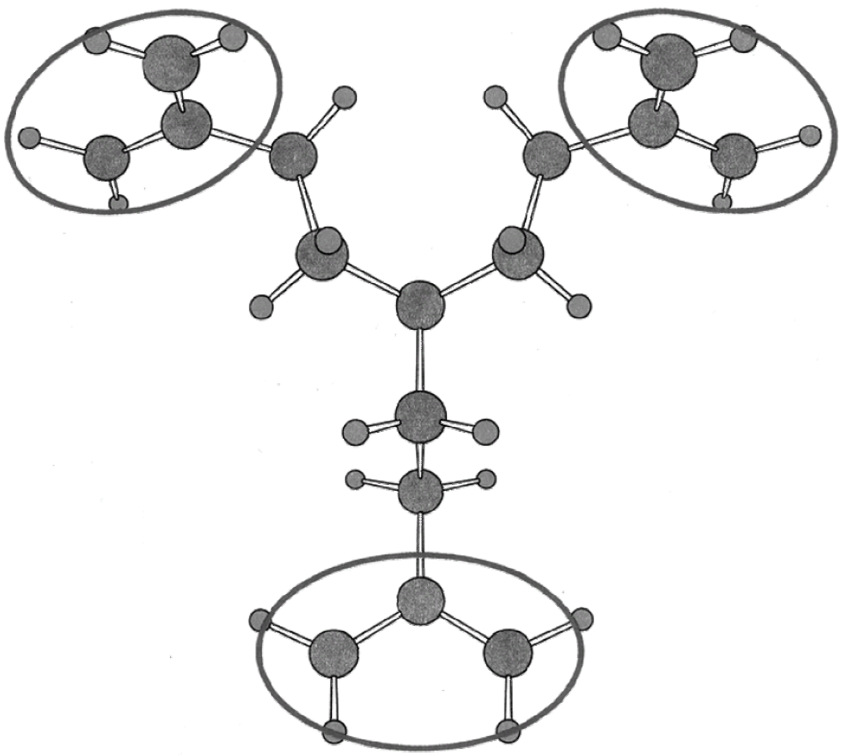
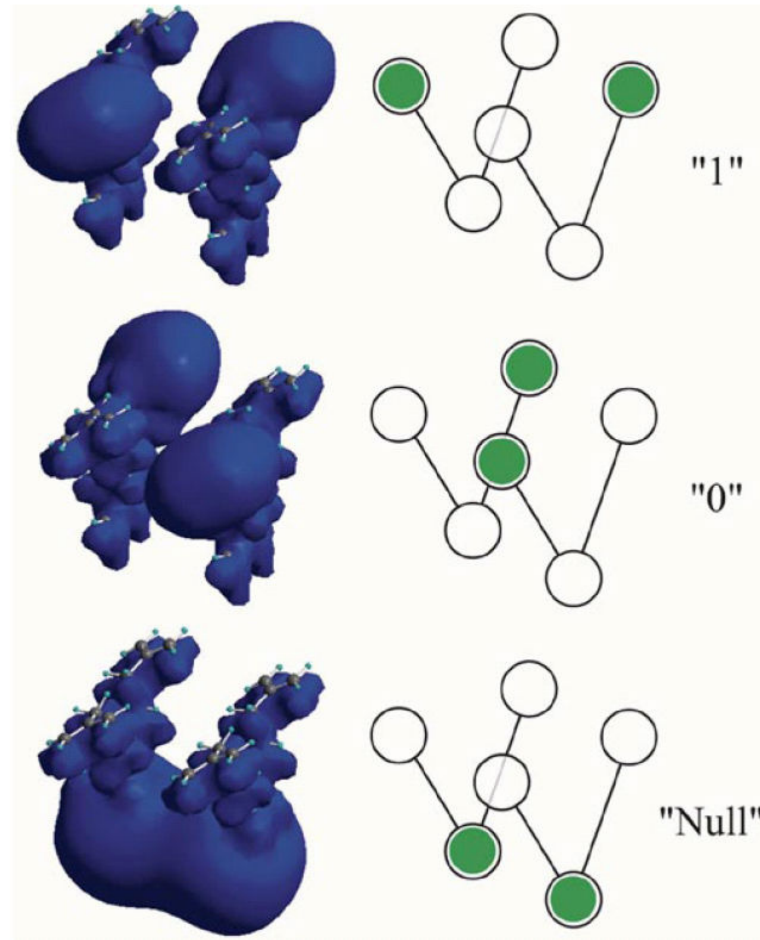
An Exemplary Device: Quantum Dots

- **Pairs of molecules create a memory cell or a logic gate**

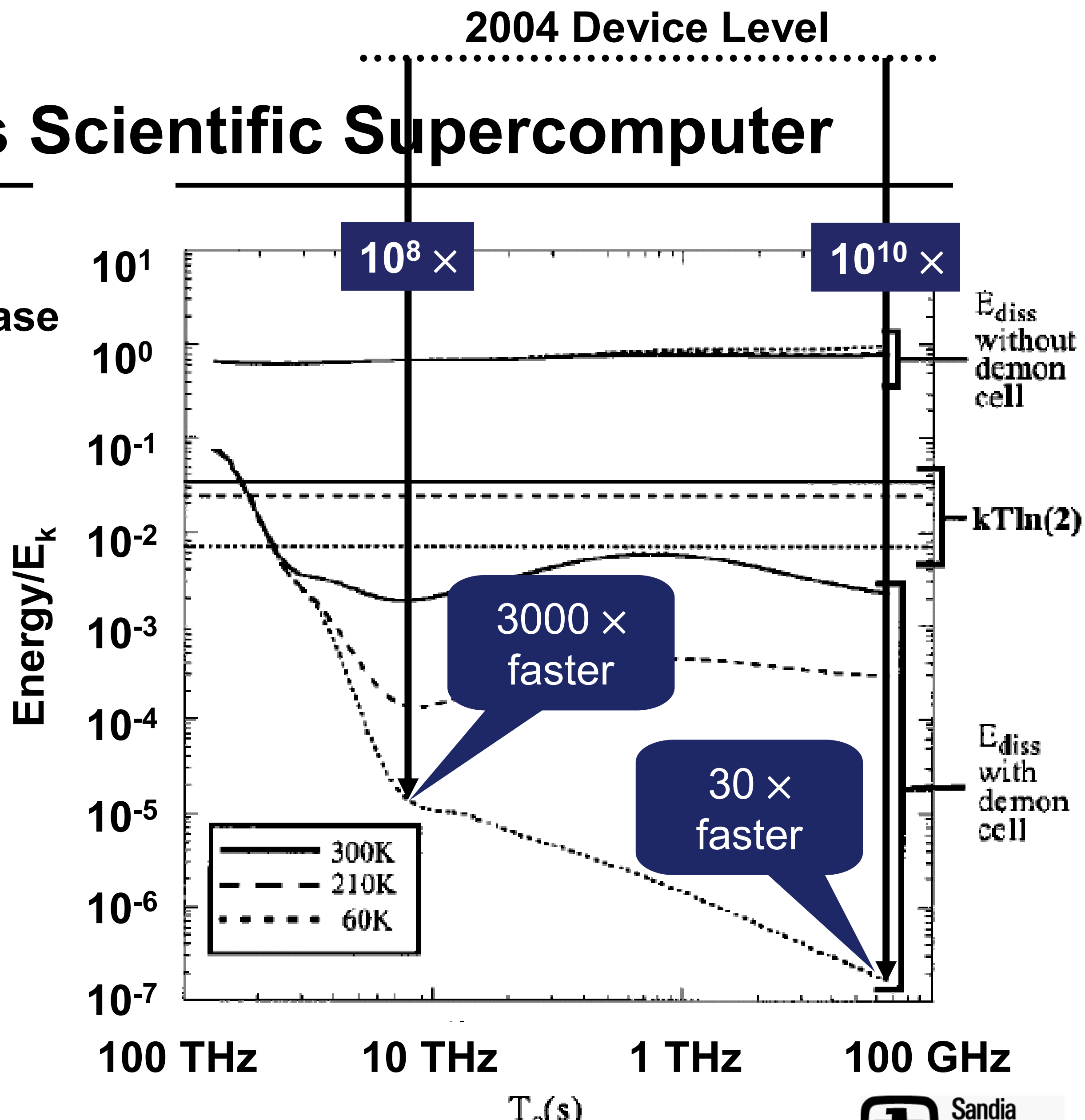




Ref. "Clocked Molecular Quantum-Dot Cellular Automata," Craig S. Lent and Beth Isaksen
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 9, SEPTEMBER 2003

1 Zettaflops Scientific Supercomputer

- How could we increase "Red Storm" from 40 Teraflops to 1 Zettaflops?
- Answer
  - $>2.5\times10^7$ power reduction per operation
  - Faster devices $\times$ more parallelism $>2.5\times10^7$
  - Smaller devices to fit existing packaging



Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent, JOURNAL OF APPLIED PHYSICS 15 JULY 2003

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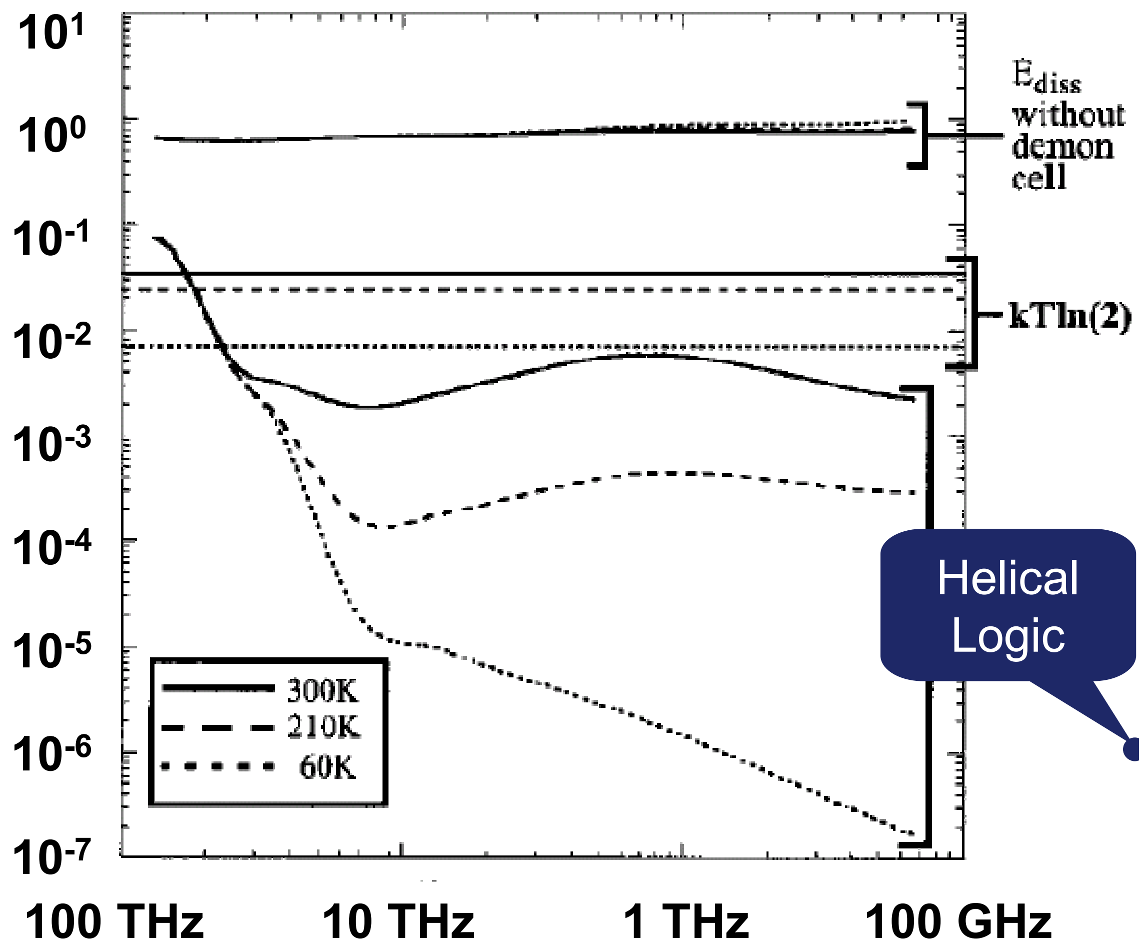
Not Specifically Advocating Quantum Dots

- A number of post-transistor devices have been proposed
- The shape of the performance curves have been validated by a consensus of reputable physicists
- However, validity of any data point can be questioned
- Cross-checking appropriate; see →



Ref. "Maxwell's demon and quantum-dot cellular automata," John Timler and Craig S. Lent, JOURNAL OF APPLIED PHYSICS 15 JULY 2003.
Ref. "Helical logic," Ralph C. Merkle and K. Eric Drexler, Nanotechnology 7 (1996) 325–339.

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QCA Microprocessor Status

- M. Niemier Ph. D. Thesis, University of Notre Dame
- 12 Bit μP
- CAD design tool principles
  - 10× circuit density of CMOS at same λ
- Applies to various devices
  - Metal dot 4.2 nm^2
  - Molecular 1.1 nm^2

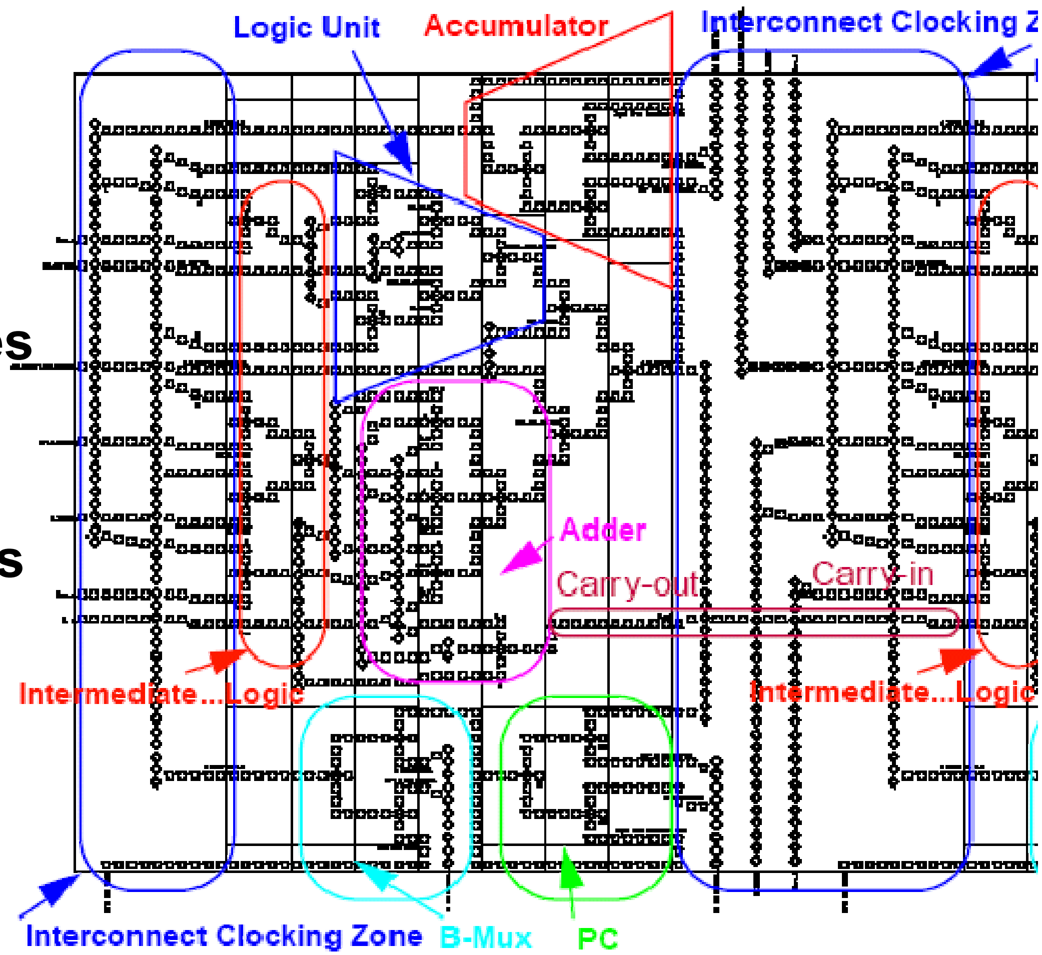

Figure 4.6. A 2-bit QCA Simple 12 ALU with registers

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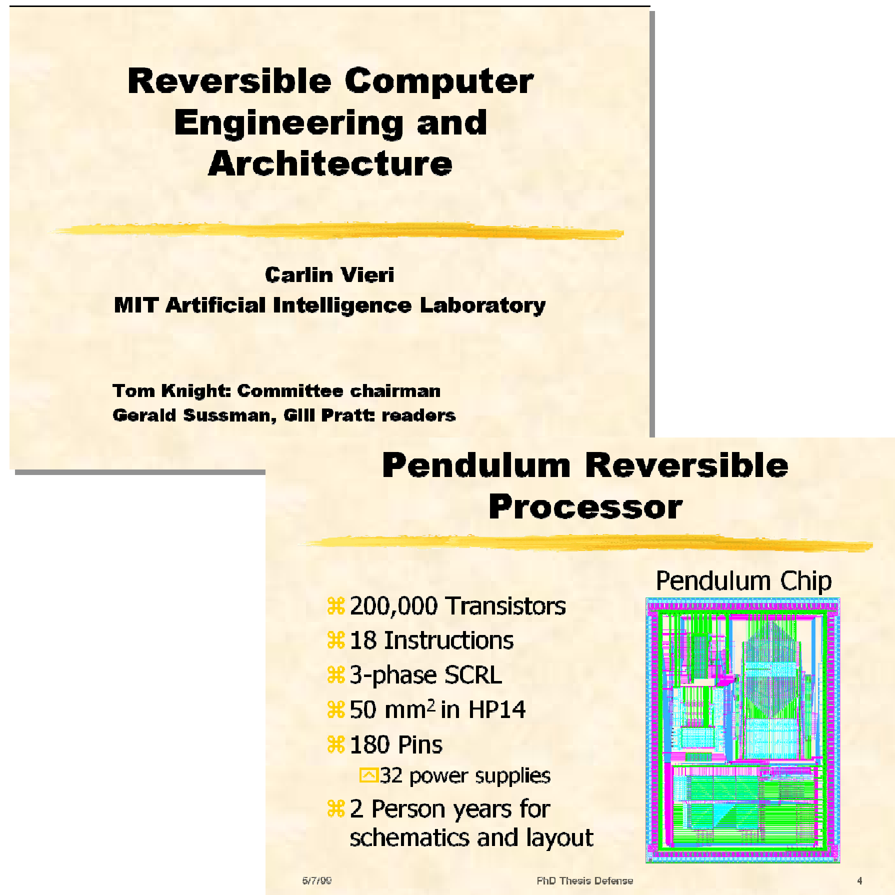
Reversible Microprocessor Status

- Status
  - Subject of Ph. D. thesis
  - Chip laid out (no floating point)
  - RISC instruction set
  - C-like language
  - Compiler
  - Demonstrated on a PDE
  - However: really weird and not general to program with +=, -=, etc. rather than =



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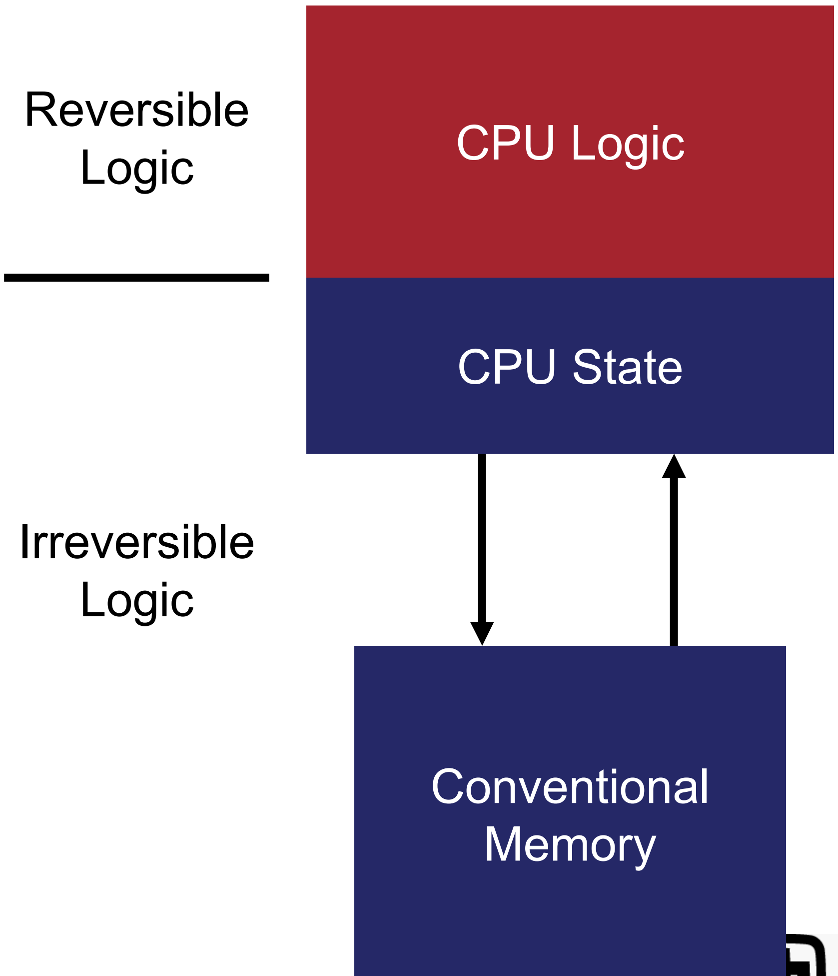
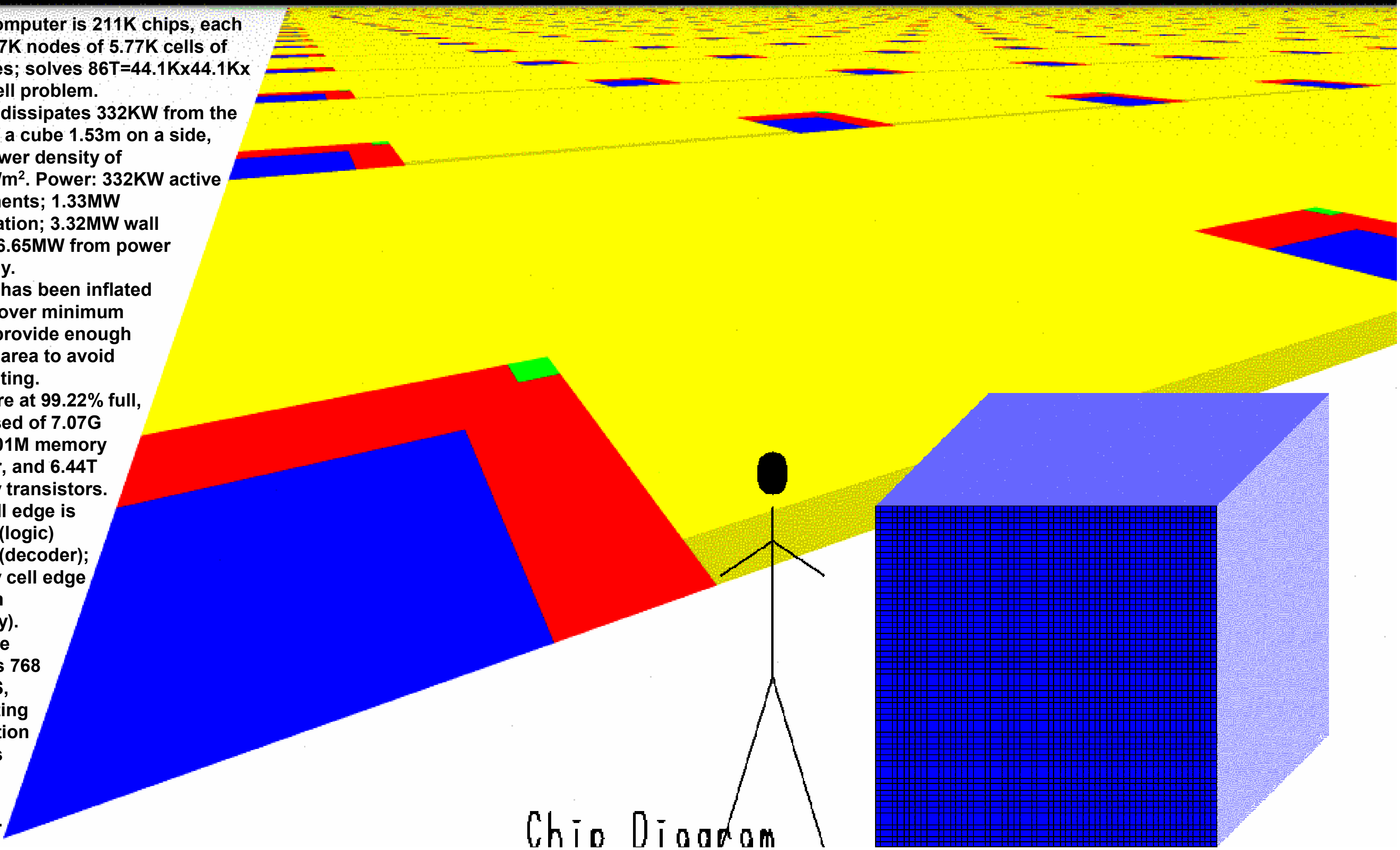
CPU Design

- **Leading Thoughts**
  - **Implement CPU logic using reversible logic**
    - **High efficiency for the component doing the most logic**
  - **Implement state and memory using conventional logic**
    - **Low efficiency, but not many operations**
  - **Permits programming much like today**

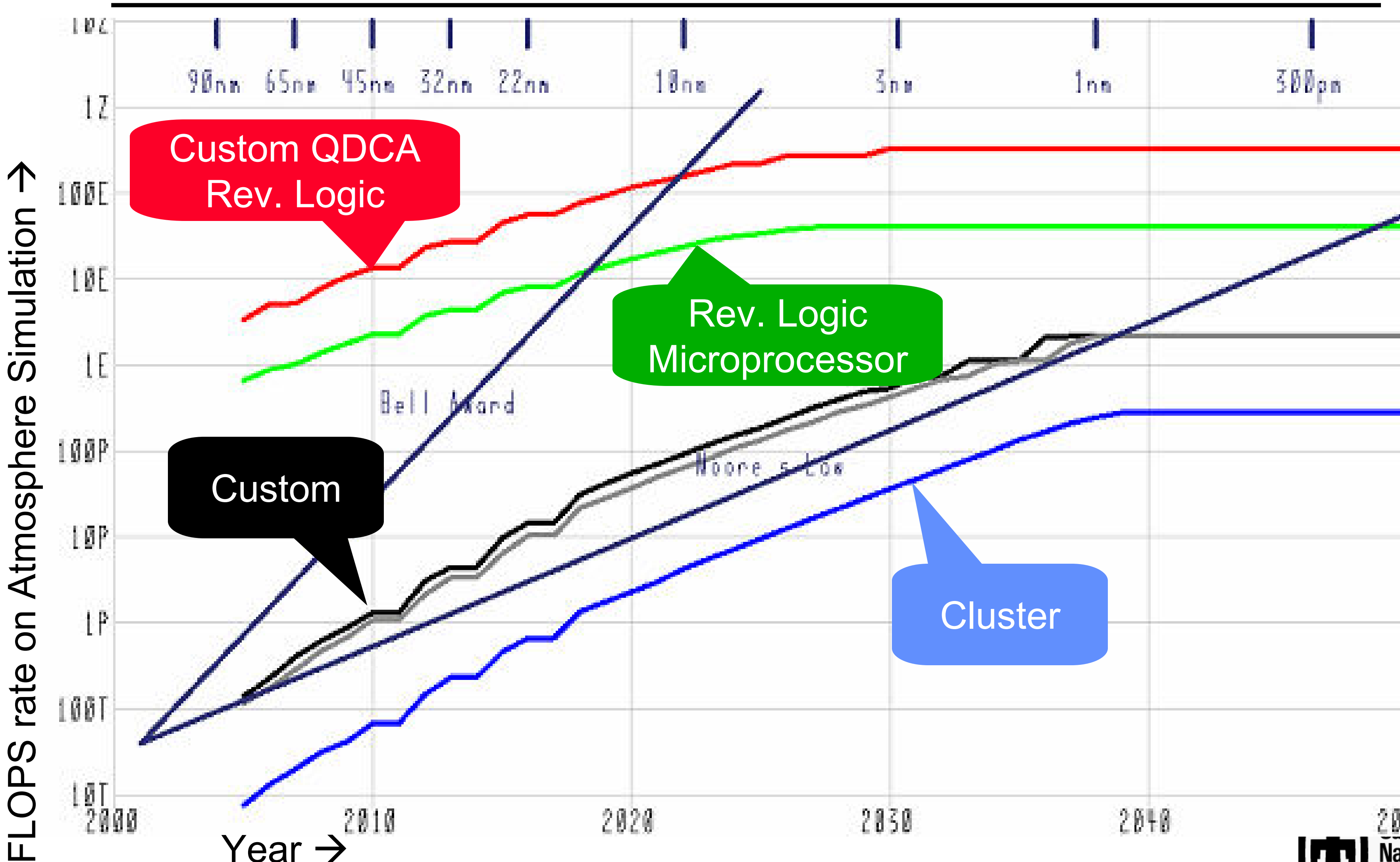


Atmosphere Simulation at a Zettaflops

Supercomputer is 211K chips, each with 70.7K nodes of 5.77K cells of 240 bytes; solves 86T=44.1Kx44.1Kx 44.1K cell problem.
System dissipates 332KW from the faces of a cube 1.53m on a side, for a power density of 47.3KW/m^2. Power: 332KW active components; 1.33MW refrigeration; 3.32MW wall power; 6.65MW from power company.
System has been inflated by 2.57 over minimum size to provide enough surface area to avoid overheating.
Chips are at 99.22% full, comprised of 7.07G logic, 101M memory decoder, and 6.44T memory transistors.
Gate cell edge is 34.4nm (logic) 34.4nm (decoder); memory cell edge is 4.5nm (memory).
Compute power is 768 EFLOPS, completing an iteration in 224μs and a run in 9.88s.



Performance Curve



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Conclusions

- There are important applications that are believed to exceed the limits of irreversible logic
  - At US$100M budget
  - E. g. solution to global warming
- Reversible logic & nanotech point in the right direction
  - Low power
- Device Requirements
  - Push speed of light limit
  - Substantially sub-$k_B T$
  - Molecular scales
- Software and Algorithms
  - Must be much more parallel than today
- With all this, just barely works
- Conclusions appear to apply generally